Video Genie System

£5-95

SERVICE
MANUAL

BY EACA

PREFACE

This manual is written for servicing technicians and people who are interested in modifying the machine to suit their particular applications. Readers are assumed to have a basic background on digital electronics and microprocessors.

The operation of each functional block will be described. Troubleshooting flowcharts are provided, however, these flowcharts should be treated as guides rather than rules.

If any error is discovered in this manual, please inform us.

CONTENTS

1. INTRODUCTION

The block diagram of the system is shown in Fig. 1. It is divided into 6 blocks, namely, CPU, RAM, Video interface, Cassette interface, address decoder and a BASIC interpreter resident in ROM. Functions of each block will be discussed in latter sections. A CPU board, an interface board, a keyboard, a cassette recorder and a power supply unit join together to form the hardware of the computer. CPU, RAM, ROM and address decoder are located on the CPU board. The other interface circuits (Video and Cassette interfaces) are on the interface board.

Fig. 1 SYSTEM BLOCK DIAGRAM
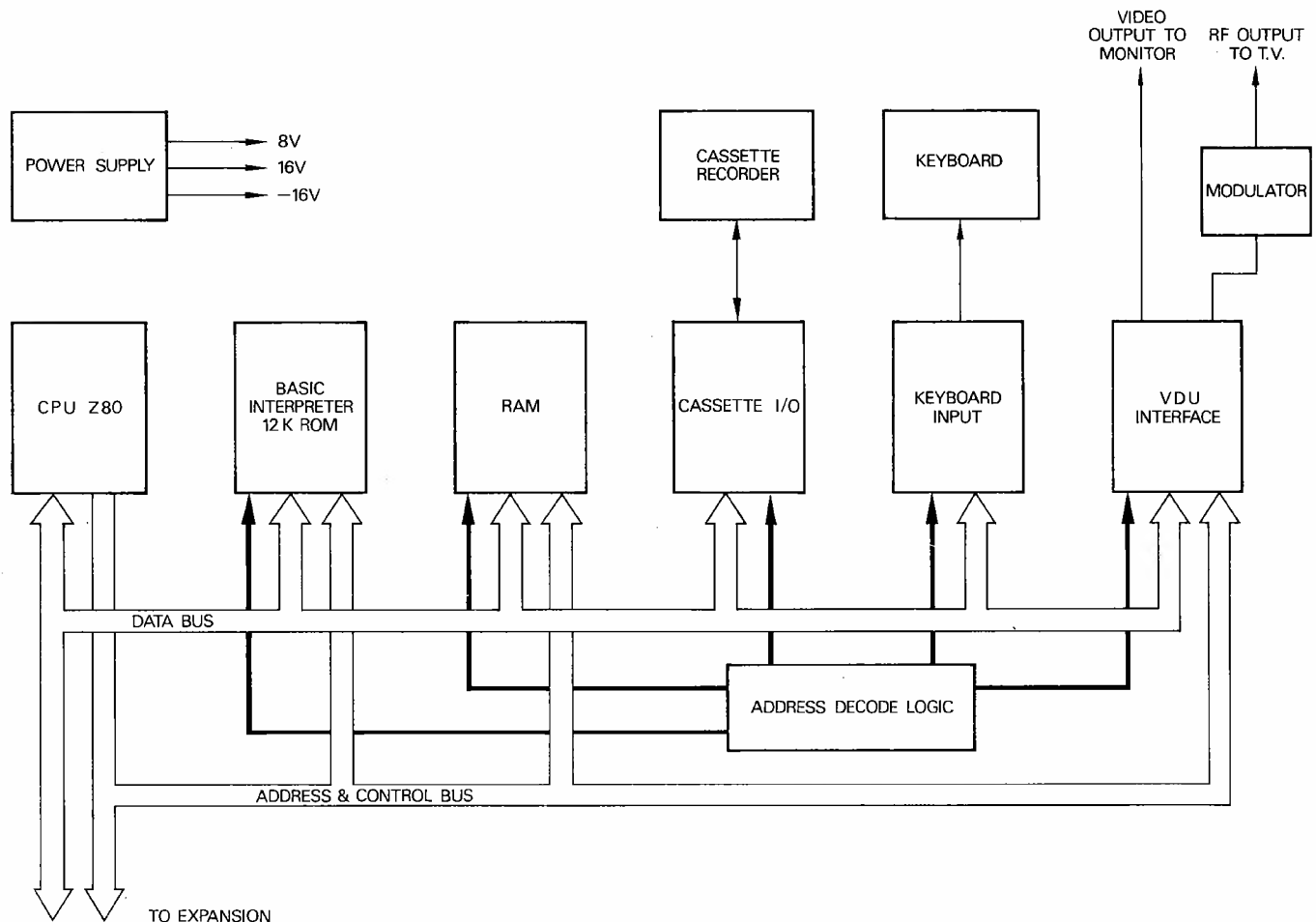
1.1 CPU

If you are already familiar with the Z80, you may go on. Otherwise, please consult the Z80 CPU technical manual.

1.1.1 CPU Clock

A master clock frequency of 10.6445 MHz is generated by a crystal oscillator. This circuit, is composed of two TTL inverters (Z31 on interface board) and a series resonant crystal. The 10.6445 MHz signal then goes into Z38 on the CPU board and is divided by six to produce a CPU clock signal of 1.77 MHz.

1.1.2 Power-on reset and system reset

Initially, the electrolytic capacitor C2 is discharged, When the power is turned on, pin 5 of Z1 is at zero volt. Hence, the output at pin 6 of Z2 is also a low level and the RESET input of the Z80 is pulled low. This initialises the CPU and sets its program counter to location zero. The capacitor is gradually charged to over 1.8 V. Pin 6 of Z2 goes high, then the CPU starts execution from address 0000 H.

The reset switch is used to get the CPU back on the right road when it is lost. When the switch is closed, pin 8 of Z2 goes low. Then, the CPU is nonmaskable-interrupted and restarts at location 0066 H. This location is another entry point to the BASIC but it does not alter any information or variable previously stored. On the other hand, entering BASIC from location 0000 H causes initialization of the whole system.

1.1.3 Address Bus

The address bus is buffered by Z4, Z6, and Z17. These buffers can supply current to drive the other circuits while the fanout of the Z80 is not capable. It can also isolate the CPU from the circuit by pulling the ADDBS/DODBS (pin 44 of edge connector) to a low level.

1.1.4 Data Bus

The data bus is also buffered like the address bus, but it is buffered bidirectionally. During the READ state, the input buffers are enabled while the output buffers are disabled. Otherwise, the action is reversed. The output buffers are also disabled when the ADDBS/DODBS is pulled low.

1.1.5 Control Bus

The control bus is buffered by Z16 and decoded by Z15 to give MWR (memory write), MRD (memory read), IN (I/O input) and OUT (I/O output).

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1.1.6 Address decoder

Z22, Z25, Z35 and Z21 decode the address bus and enable the corresponding device.

The following table shows the relationship between the address lines and the enabled devices.

A15	A14	A13	A12	A11	A10	Enabled device	Decoded O/P
0	0	0	0	X	X	ROM 1	Z22 pin 9, 10
0	0	0	1	X	X	ROM 2	Z22 pin 11, 12
0	0	1	0	X	X	ROM 3	Z22 pin 7, 6
0	0	1	1	1	0	Keyboard	Z35 pin 11
0	0	1	1	1	1	Video RAM	Z35 pin 3
0	1	0	0	X	X	4K RAM	Z25 pin 4
0	1	X	X	X	X	16K RAM	Z25 pin 11

X means don't care.

Fig. 2.

MEMORY MAP

FFFF	
	FOR EXPANSION
7FFF	
	16K RAM
3C00-3FFF	VIDEO DISPLAY MEMORY
3800-37FF	RESERVED FOR KEYBOARD
2FFF	
0000	

I/O PORT ASSIGNMENT

CASSETTE INTERFACE — FF, FE

PRINTER INTERFACE — FD

1.2   RAM

The EG3004 has 4K bytes built-in RAM whilst the EG3003 has 16K bytes. Upgrading the EG3004 to 16K can be done by changing the RAM chips together with proper setting of the jumper X1. The RAMS used are dynamic type. They need periodic refreshing in order to retain the stored data. Three control signals: MUX, RAS and CAS are associated with the RAM operation.

1.2.1 MUX, RAS and CAS

Normally, a 16K memory requires 14 address lines, but in our system, only 7 lines are used. Those 14 lines are divided into 2 groups and are multiplexed to the address lines of the RAM. When MUX is low, A0 − A6 are gated to the outputs of multiplexer Z23, pin 4, 7, 9, 12 and Z24, pin 4, 7 and 9. This low order address is latched into the RAM chips as the row address when RAS goes from high to low. When MUX is high, the higher order address, A7 − A13, is latched into the memory chips as the column address.

Refer to the schematic, RAS is the same signal as the MREQ at pin 19 of the CPU chip.
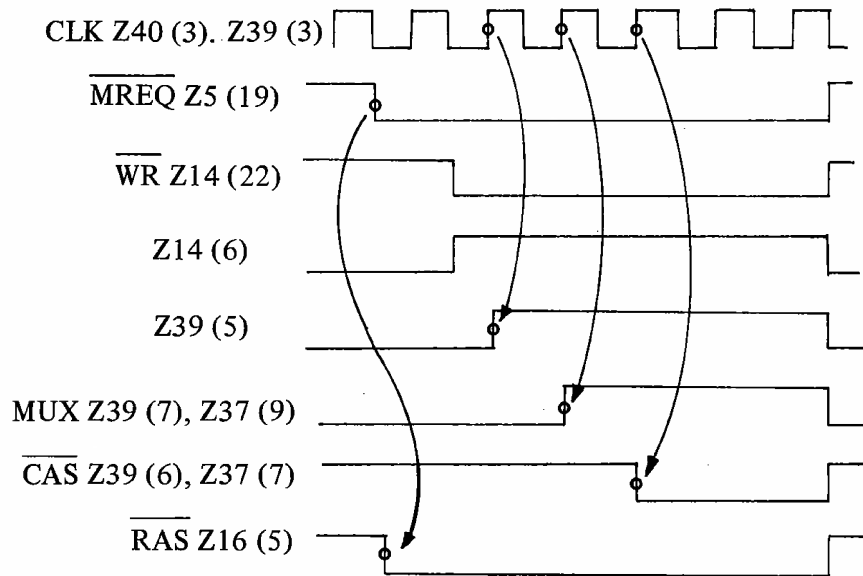
Fig. 3.

Fig 3 shows how the MUX and CAS signals are generated by Z39, Z40 and Z14. Both Z39 and Z40 are driven by the system clock generator. When either the WR of the RD is active (low), the Z14 NAND gate gives a high output. This is connected to the D-input (pin 2) of Z40. The three D-type flip-flops of Z39 and Z40 form a synchronized delay counter. The MUX obtained at Z39 pin 8 is the input signal delayed by 2 clock cycles. After one more clock cycle, the active low CAS signal is obtained from Z39 pin 6. When WR or RD goes high again (inactive), pin 6 of Z14 goes low, the 3 D-type flip-flops are reset and MUX, RAS and CAS signal are reverted to their initial inactive states.

1.2.2 Memory Read and Write

During memory read, pin 8 of Z21 goes low and the buffers (Z9 and Z20) are enabled. The RAS signal strobes the row address into the RAMS. The coming CAS strobes the high order address and CE signal into the RAMS. The data inside the RAMS will then get onto the data bus through the buffers. CAS is also used for chip selection and address strobing. The CAS signal is gated through a buffer (Z35). The buffer enable input (pin 15) is connected to pin 11 of Z25.

The memory write cycle is similar to the read cycle. The only difference is that the WR input (pin 3) of the RAM, which is connected to MWR, is at a low level. Also, the buffers are disabled.

1.2.3 Refreshing the RAMS

After each instruction fetch, the Z80 places a refresh address on its address bus with the MREQ (RAS) low at the falling edge of T3 clock state. This address is latched into the dynamic RAM chips by the RAS, and is used for refreshing the addressed row of memory. The address will be incremented by one in the next refresh cycle.

1.3   VIDEO INTERFACE

In this section, we will trace the circuit in a reverse order, that is, back from the output end to the input. We will discuss, how the composite Video is produced, then, how to generate the timings for Video RAM scanning, also, how to convert data in the RAM to Video information and lastly, how to change the data in the Video RAM.

Fig. 4.   VIDEO INTERFACE BLOCK DIAGRAM
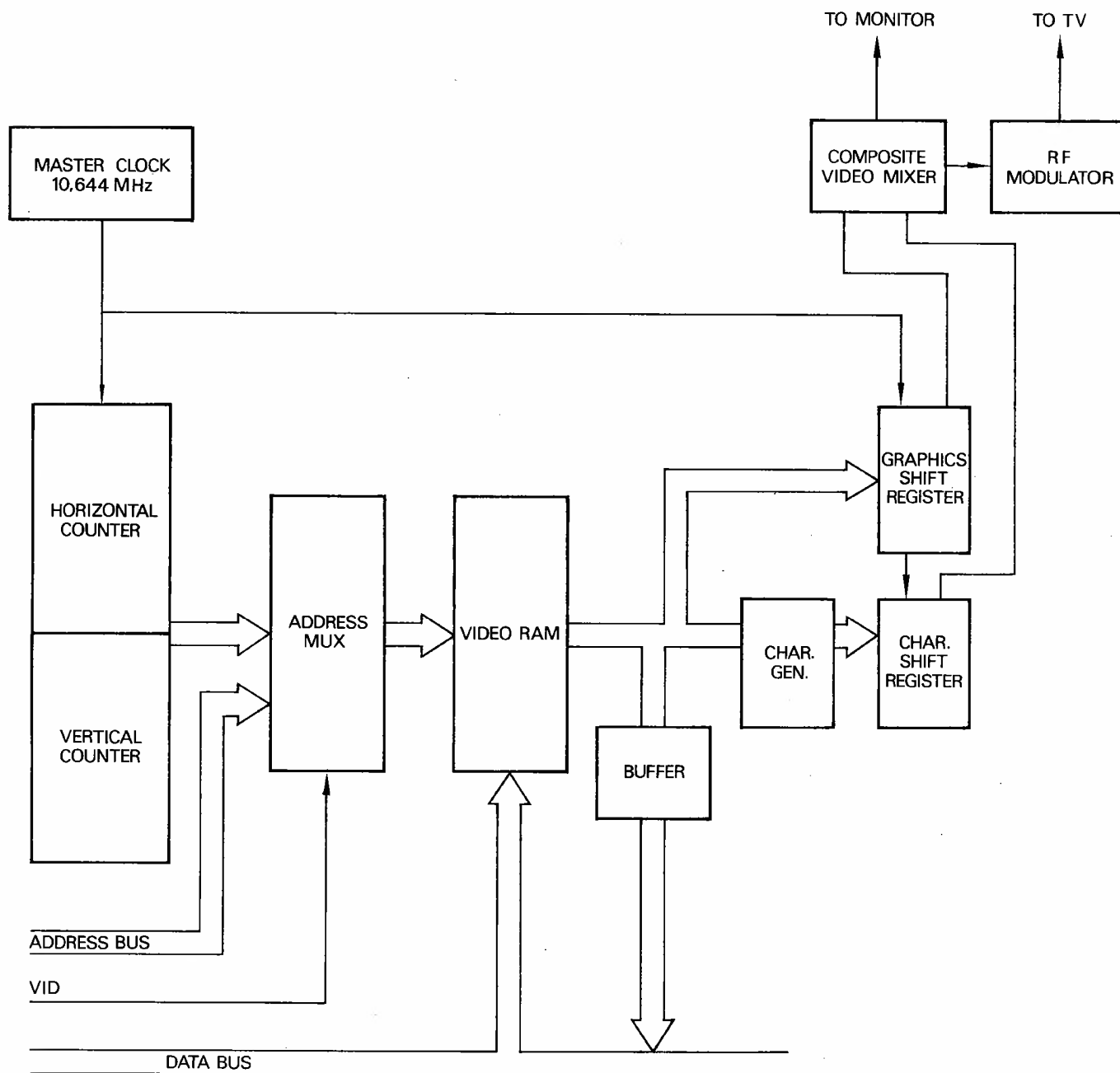
1.31 Sync signals

At the present stage, we will just discuss the timings for 64 characters/line format and leave the 32 characters/line format in the latter section.

The horizontal and vertical frequencies are obtained by dividing the master clock through a counter chain. The output frequencies at Z34 (11)* and Z32 (11) are the horizontal and vertical sync frequencies. However, the waveforms at these outputs do not meet the specifications of sync signals. These two signals are then fed into a reshaping circuit. Z1 and Z10 do the job. VR1, C17 and two inverters of Z1 delay the horizontal signal from Z34, while VR2, C16 and the other two inverters of Z1 delay the vertical signal from Z32. Therefore when we adjust the VR1 or VR2, the horizontal position or vertical position of the picture can be shifted. C18, R12 and Z10 acts as a monostable, and similarly, C19, R11 and the other inverter of Z10 is another monostable. The monostable will output a pulse whenever its input turns from low to high. The pulse width depends on the RC time constant. Finally, horizontal sync pulses from pin 10 of Z10, while vertical sync pulses output from pin 4 of Z10. Z22 which forms an exclusive OR gate combines the horizontal and vertical sync signals.
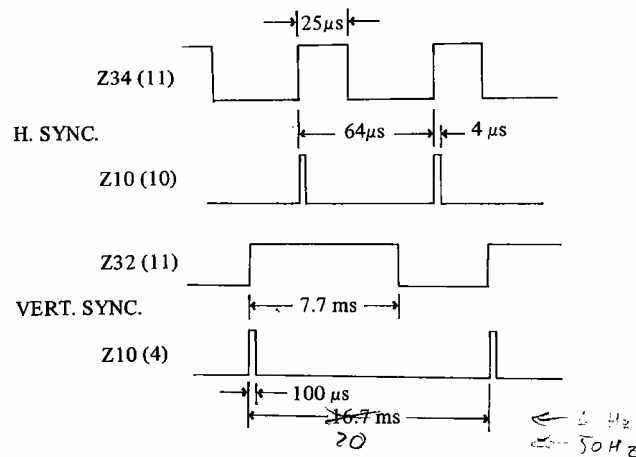
Fig. 5.   SYNC. GENERATOR TIMING

* Note:– Z34 (11) means pin 11 of Z34.
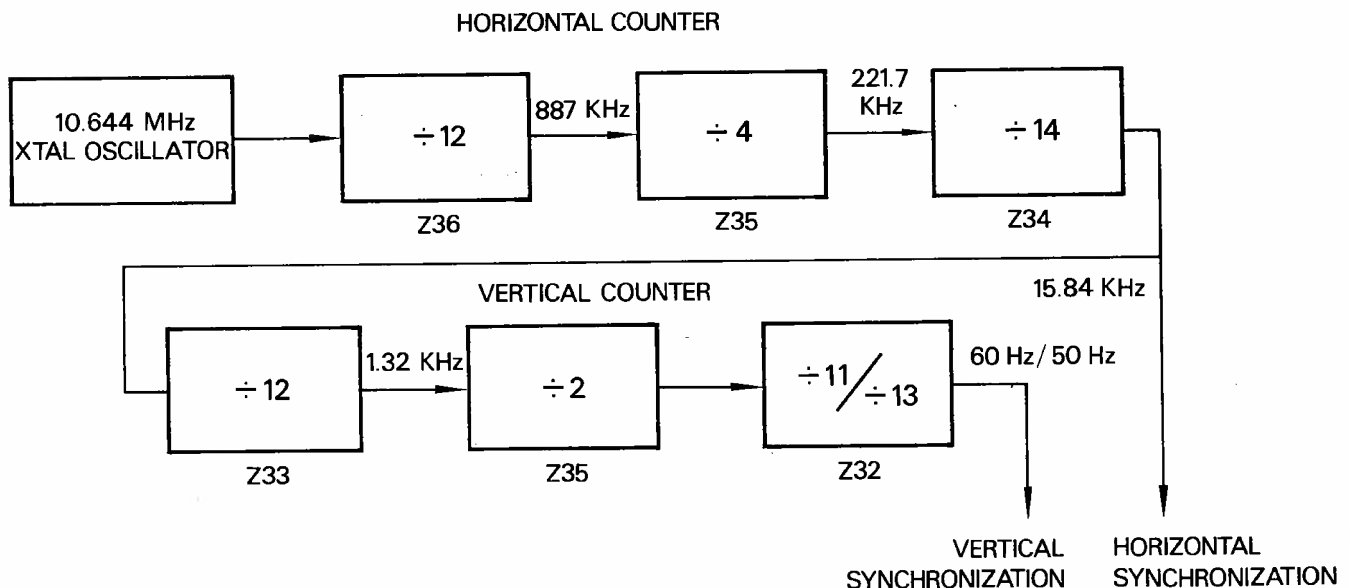
Fig. 6.

1.3.2 Mixing of synchronization and video signal

Assuming that the video and the sync signals already exist. The video signal outputs from pin 4 of Z11 while the composite sync signal outputs from pin 11 of Z22. These two signals are then mixed up by Q1, Q2, and Q3 to give the composite video. The three transistors act as three switches.
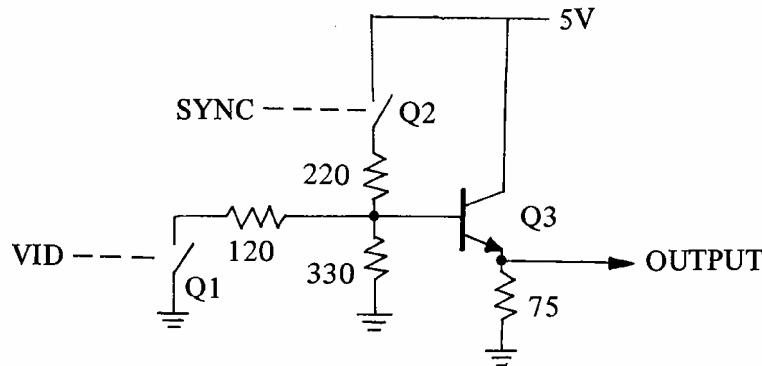
Equivalent circuit of Video mixer

1.3.3 Video RAM addressing

We have discussed that the horizontal and vertical counters are used to produce the sync frequencies, but the other outputs of the counters are also used to address the Video RAM.

Since the System displays 64 characters per line and each character corresponds to one ASCII code stored in one memory location, 64 video memory location should be accessed in sequence during the scanning of each line. Each row of characters occupies 12 scanning lines, therefore, the vertical address increases by one every 12 lines.

Now, let us look at which outputs of the counters are connected to the RAM's address lines through multiplexers Z29, Z30, Z34 and Z37.

Horizontal	Address	Vertical	Address
Z36 pin 8	A0	Z32 pin 14	A6
Z35 pin 9	A1	Z32 pin 12	A7
Z35 pin 8	A2	Z32 pin 9	A8
Z34 pin 12	A3	Z32 pin 8	A9
Z34 pin 9	A4		
Z34 pin 8	A5		

If the CPU wants to access the video RAM, a VID signal, which outputs from the address decoder, goes low. The multiplexers Z30, Z29 and Z38 switch from the horizontal and vertical address to the CPU's address bus. Then, the RD signal will enables the output buffers of the video RAM and gets data onto the data bus. At the write mode, the WR signal will set the RAM's R/W line low and store data on the data bus into the RAM.

There are only seven 2102 instead of eight pieces. The most significant bit, d_7 (Z12) controls the display mode, one represents Graphics mode while zero represents character mode.

1.3.4 Generation of Video Signals

Before discussing the operation of the circuits, we should look at the display formats. In alphanumeric mode, each row of character is composed of 12 scanning lines. Out of that 12 lines only 8 contains information and the other four are blanked. In the graphic mode, each row consists of 64 units and each unit is made up by 6 dots. Each dot corresponds to one data bit in the RAM. (See Fig. 9).

In each row of characters the line number of the 12 line may be represented by 4 bits. Let us call these 4 bits L0, L1, L2 and L3. They are output from pin 12, 9, 8 and 11 of Z23 respectively. For example, when line 6 of a row is scanning, (L3, L2, L1, L0) is (0, 1, 0, 1).

Now, let us analyse how an alphanumeric character is loaded into the shift register and shifted out as video signal. When the divide-by-six counter Z36 counts to 5, pin 3 of Z28 goes low. The occurance of this signal causes two actions.

1. The outputs from the character generator Z25 is loaded into Z4.
2. During the rise edge, the status and data of the next character are latched by Z3 and Z26.

The data stored in the shift register is then shifted out by the 10.644 MHz pulse again. Then, the 2 actions mentioned above repeat again and the next character is shifted out.

The character generator is addressed by the 6 data bits in RAM and the line counter (L3, L2, L1, L0). Since line 8-11 of each row of characters have to be blanked, the output pin 11 of Z3 is the latched status of line blanking. When this output is low, data loading into the character shift registers is inhibited. Similary, output pin 15 is the vertical and horizontal blanking signal. It is the ORed signals of most significant bits of vertical and horizontal counters.

Fig. 7. VIDEO DISPLAY TIMING OF A CHARACTER
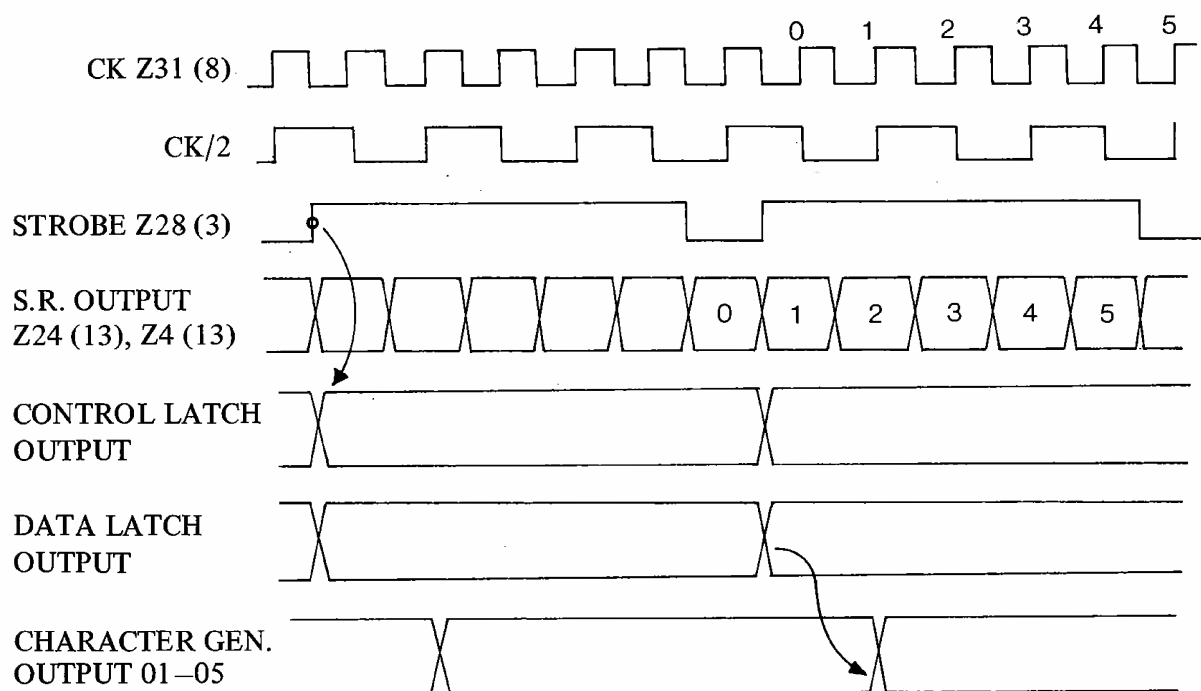
Fig. 8. VIDEO DISPLAY TIMING OF A LINE

Horizontal counter address: 0 1 2 3 4 ... 63 64

Output Z3 Control latch: 0 1 2 3 ... 62 63 64

Output Z26 Data latch: 0 1 2 3 ... 62 63

Shift register Output Z4, Z24: 0 1 2 ... 62 63
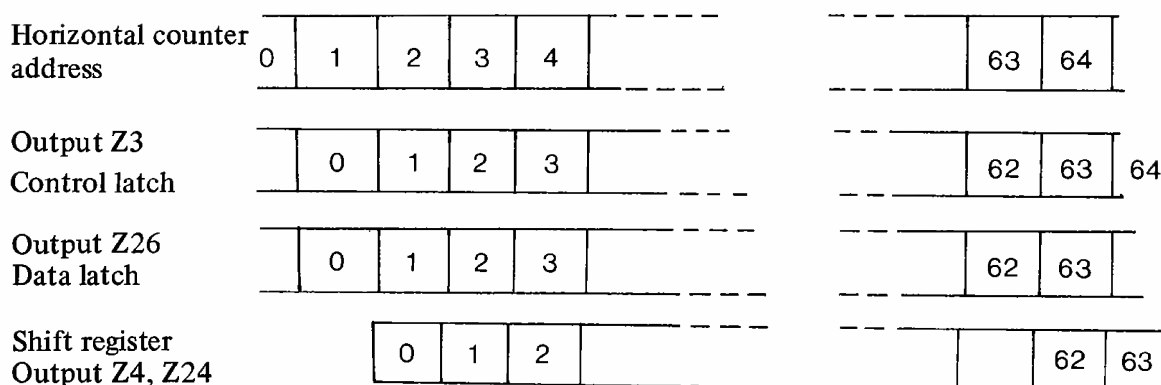
* The numbers in the control and data latches timings represent the control signals or data of the corresponding horizontal address.

line ∅

11

	Character mode	Graphic mode
Ram data	0 x 00001	1 x 010101
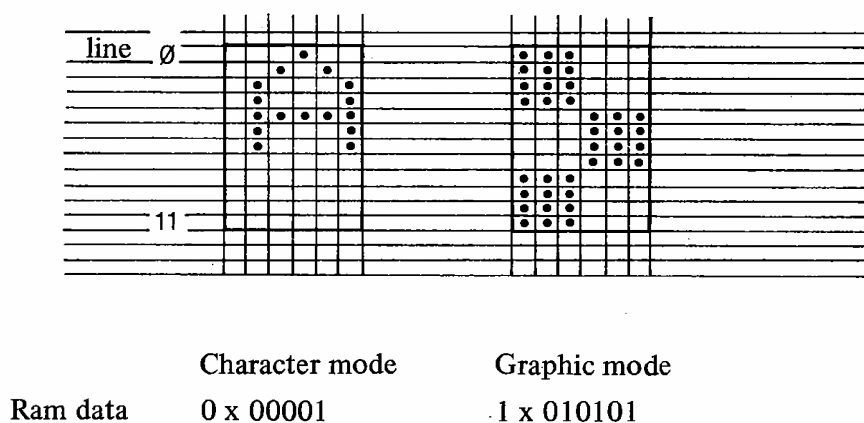
Fig. 9. DISPLAY FORMAT

1.3.5 32 characters/line

In the 32 characters/line mode, switch S1 is closed. The multiplexers Z29 and Z37 are then switched to the other side. Originally, A0 of the video RAM is connected to pin 8 of Z36 through the mux, but now, it's connected to pin 9 of Z35. Similarly, A1 is connected to the former A2, A2 to A3; A3 to A4, and A5 to the PAGE switch. If page is zero, left page is accessed, otherwise, right page will be accessed. The data strobe timing is also scaled down by 2. This is done by feeding CK/2 signal to Z36.

1.3.6 Graphic mode

The interface is in graphic mode when the most significant bit of the video RAM is one. This bit is latched by Z3 at the same time when the other 6 bits are latched by Z26. The latched D7 disables the upper NAND gate of Z2 and enables the lower one. The next data strobe signal will load the data into Z24. Since only two data bits will be loaded into Z24, Z24 selects two bits from those six each time. The selection is controlled by L2 and L3. At scanning lines 0–3, D0 and D1 are selected. At lines 4–7, D2 and D3 are selected and at lines 8–11, D4 and D5 are selected.

A GRAPHIC CELL

d0	d1
d2	d3
d4	d5

1.4 CASSETTE INTERFACE

The cassette interface uses port FF and FE for its I/O and control. These two addresses are decoded by Z19 and Z20.

The following table shows the bit assignments of the ports.

	High	Low
Output Port FF D2	Cassette ON	Cassette OFF
D1, D0	signal output	
Input Port FF D7	signal input	
Output Port FE D4	Cassette 2 select	Cassette 1 select

1.4.1 Cassette Selection

Normally, pin 8 of Z40 is at high level. If the cassette ON/OFF signal at pin 2 of Z6 is one, REL1 will be switched on. When the CPU wants to select cassette 2, it turns D4 of port FE to high. Therefore, Q output of Z40 (pin 9) goes high and Q (pin 8) goes low. REL 2 is switched ON and REL1 is OFF. As a result, the remote switch of cassette 2 closes and its input and output lines are connected to the interface circuit.

1.4.2 Cassette write

The waveform shown in Fig. 10 is generated by toggling bits D1 and D2 of port FF. These two bits output at pin 11 and 15 of Z6.

Fig. 10.   CASSETTE WRITE TIMING
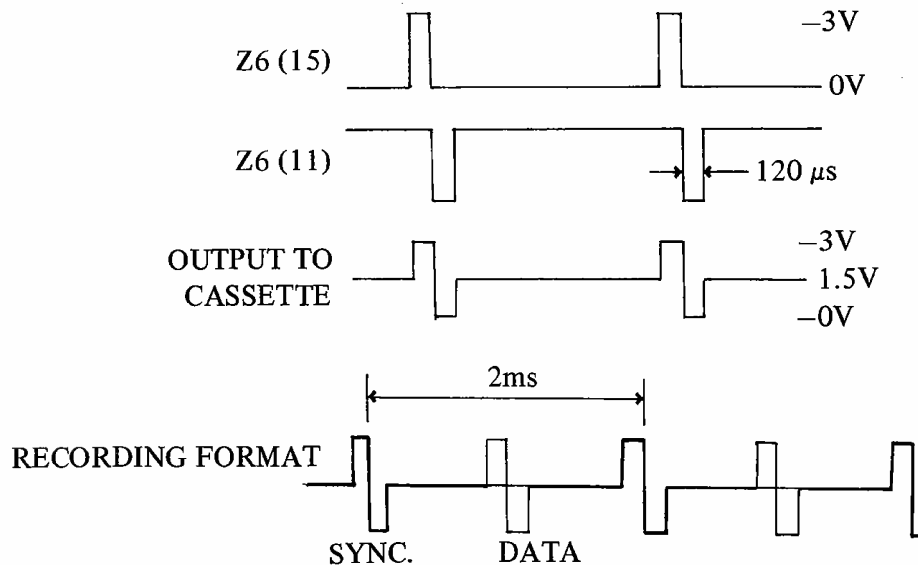
1.4.3 Cassette read

The incoming signal is shaped by Z9. Firstly, it passes a high pass filter to eliminate hums. Then the signal is inverted. The output signals at pin 8 and 14 of Z9 are then rectified to get their lower cycles. The rectified signal then goes to a comparator and will be shaped into square pulses. The pulses then goes to pin 9 of Z28, and trigger the R-S flip-flop formed by two NAND gates of Z28. The output of the flip-flop will then be read back to the CPU through bit 7 of input port FF.

After the CPU has detected a 1 at the flip-flop output. It will reset the flip-flop after 500 usec. If the pulse is a sync pulse, the CPU will sample the data after 1 msec and reset the flip-flop. Waveform at pin 8 of Z29 is delayed for about 250 usec and output at pin 1 of Z9. The delayed signal pulls up pin 5 of Z9 and prolongs the blanking period of the incoming pulses.

Fig. 11.   CASSETTE READ TIMING
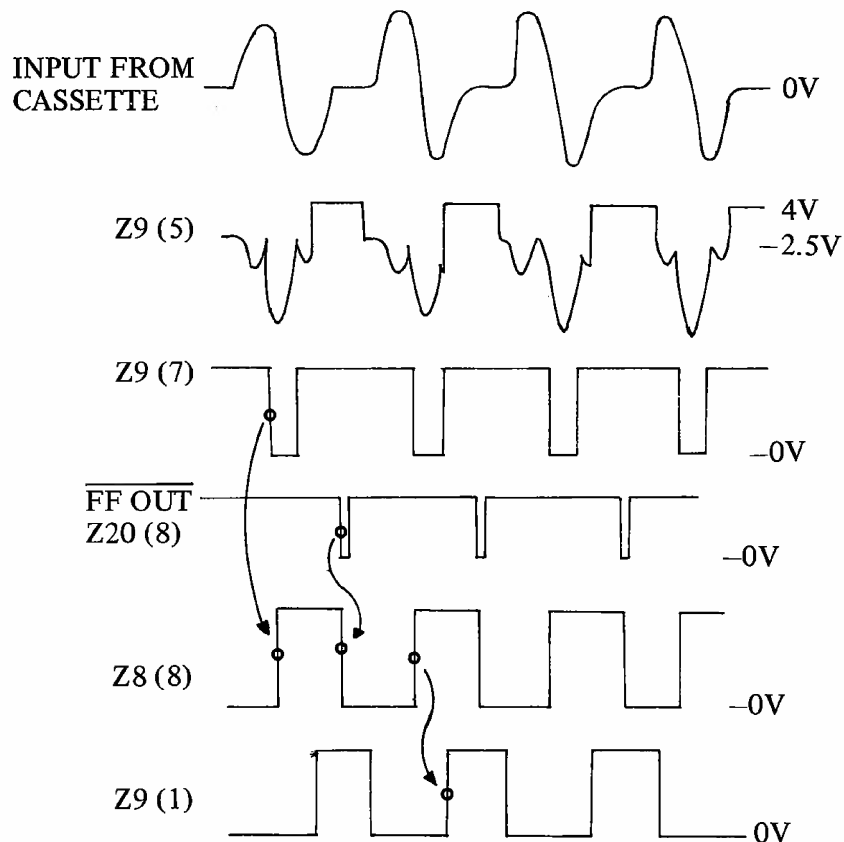
1.5   KEYBOARD

The key switches are arranged in a matrix and scanned by AK0—7 and DK0—7. AK0—7 are eight buffered address lines. The keyboard scanning input buffers are enabled when the CPU accessing memory location 3C00H—3FFFH. If the CPU wants to scan the row H—O, it reads from memory location 3C02H. If the L key is depressed, a byte 08H will be read into the accumulator. If no key is depressed, 00H will be read.

Knowing the corresponding mapped memory location and the data received, the CPU decodes the input to an ASCII code.

Two other switches, the F1 and PAGE keys, are not software scanned, but directly control the hardware of the system.

1.6 POWER SUPPLY

The power supply has three output voltages: — +8V, +16V and —16V.
The following table shows the specifications for the three outputs.

Voltage	No load voltage		Full load voltage		Remark
	min	max	min	max	
+8V	10.5V	11.5V	8V	9V	F.L. +8V @1.2A
+16V	20V	24V	15V	18V	F.L. +16V @150mA
—16V	20V	24V	15V	18V	F.L. —16V @100mA

2. TROUBLESHOOTING

2.1 TYPES OF FAULT

Three common types of fault are component failure, open circuit and short circuit. Since the Genie has to pass a very strict quality checking, short circuit seldom happens. Open circuit and failure of component are more common.

It may be caused by shock during transportation or running the Genie under adverse condition (eg. high temperature and high humidity).

2.2   DATA, ADDRESS AND CONTROL BUS TESTER

This simple tester disables the CPU buffers and places data, address and control signals on the buses. Therefore, short circuits and open circuits can be tested under static condition.

Tester circuit diagram.

2.3 TROUBLESHOOTING FLOWCHARTS

```
                            ┌──────────────┐
                            │    START     │
                            └──────┬───────┘
                                   │
                            ┌──────▼───────┐
                            │ CHECK POWER  │
                            │SUPPLY VOLTAGES│
                            └──────┬───────┘
                                   │
                              ◇UNSTABLE PICTURE◇  ──YES──►  ┌─────────────┐ VID 1
                              ◇ OR NO PICTURE  ◇            │    CHECK    │
                                   │                        │VIDEO INTERFACE│
                                   │                        └─────────────┘
                                   │
                              ◇  GARBAGE   ◇  ──YES──►  ┌─────────────┐ VID 2
                              ◇ ON SCREEN  ◇            │    CHECK    │
                                   │                    │VIDEO INTERFACE│
                                   │                    └──────┬──────┘
                                   │                           │
                                   │              ◇NORMAL FUNCTION◇ ──YES──
            KEY                    │                           │
   ┌──────────────┐          ◇ANY KEYBOARD◇              ┌─────────────┐ ROM
   │CHECK KEYBOARD│ ◄──YES──  ◇  PROBLEM   ◇              │  CHECK ROM  │
   └──────────────┘                │                     └──────┬──────┘
                                   │ NO                         │
            CAS                    │              ◇NORMAL FUNCTION◇ ──YES──
   ┌──────────────┐          ◇CASSETTE PROBLEM◇            │
   │CHECK CASSETTE│ ◄────────                        ┌─────────────┐ RAM
   │  INTERFACE   │                │                 │  CHECK RAM  │
   └──────────────┘                │ NO              └─────────────┘
                            ┌──────▼───────┐
                            │   FINISH     │
                            └──────────────┘
```

```
                              ┌──────────┐
                              │   VID 1  │
                              └────┬─────┘
                                   │
                                   ▼
                              ╱─────────╲                    NO
                             ╱ NO PICTURE ╲─────────────────────────┐
                             ╲            ╱                          │
                              ╲─────────╱                           ▼
                                   │ YES                      ╱──────────────╲    NO
                                   ▼                         ╱     LOSE        ╲──────┐
                         ┌──────────────────┐               ╲ SYNCHRONIZATION ╱      │
                         │ CHECK 10,644 MHz  │               ╲──────────────╱        │
                         │  MASTER CLOCK     │                      │ YES            │
                         └────────┬─────────┘                       ▼                │
                                  │                        ┌──────────────────┐      │
                                  ▼                        │     CHECK        │      │
                         ┌──────────────────┐              │ SYNCHRONIZATION  │      │
                         │  CHECK VIDEO      │              │   GENERATOR      │      │
                         │  SHIFT REGISTER   │              └────────┬─────────┘      │
                         └────────┬─────────┘                       │                │
                                  │                                 ▼                │
                                  ▼                        ┌──────────────────┐      │
                         ┌──────────────────┐              │     CHECK        │      │
                         │  CHECK VIDEO      │              │  VIDEO MIXER     │      │
                         │  DIVIDER CHAIN    │              └────────┬─────────┘      │
                         └────────┬─────────┘                       │◄───────────────┘
                                  │                                 ▼
                      YES         ▼                         ┌──────────────┐
              ┌──────────────╱─────────╲                    │    RETURN    │
              │             ╱ CHARACTERS ╲                   └──────────────┘
              │             ╲    OK     ╱
              ▼              ╲─────────╱
         ╱─────────╲              │ NO
        ╱ GRAPHICS  ╲             ▼
    NO  ╲    OK     ╱    ┌──────────────────┐
   ┌────╲─────────╱     │ CHECK CHARACTER   │
   │          │         │   GENERATOR       │
   ▼          │         └────────┬─────────┘
┌──────────┐  │                  │
│ CHECK    │  │                  ▼
│ Z 24,Z 27│  │         ┌──────────────────┐
└────┬─────┘  │         │ CHECK VIDEO RAM   │
     │        ▼         └────────┬─────────┘
     │   ┌──────────┐            │
     └──►│  RETURN  │◄───────────┘
         └──────────┘
```

```
        ╭─────────────╮
        │    VID 2    │
        ╰─────────────╯
               │
        ┌─────────────┐
        │ CHECK INTERBOARD │
        │   CONNECTOR      │
        └─────────────┘
               │
        ┌─────────────┐
        │    CHECK        │
        │ ADDRESS DECODER │
        └─────────────┘
               │
        ╭─────────────╮
        │   RETURN    │
        ╰─────────────╯
```

Remark:—
1) A system that mis-spells words usually has data screw-ups in video RAM, or the data going to character generator is being grabbed by a defect around latch Z26.
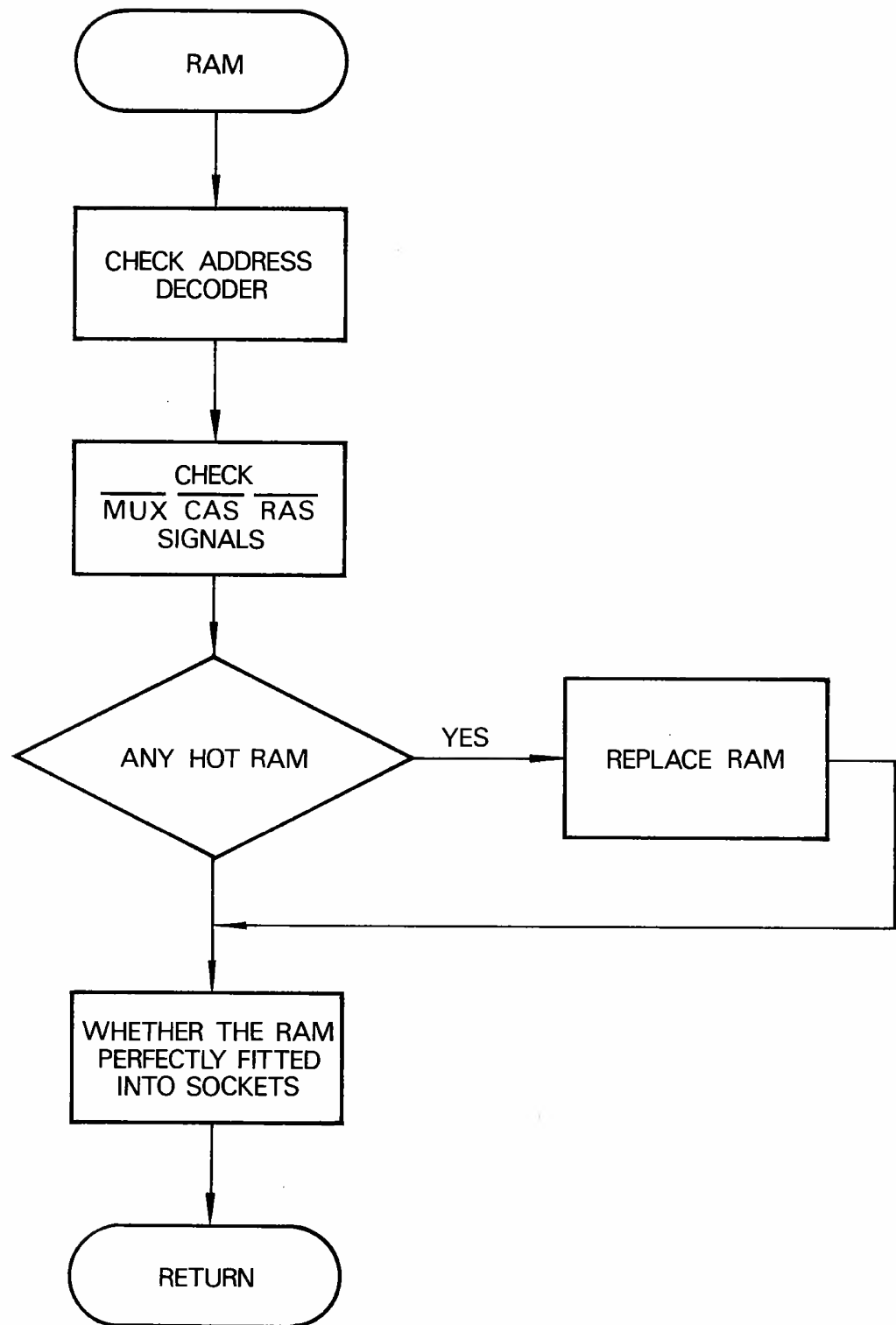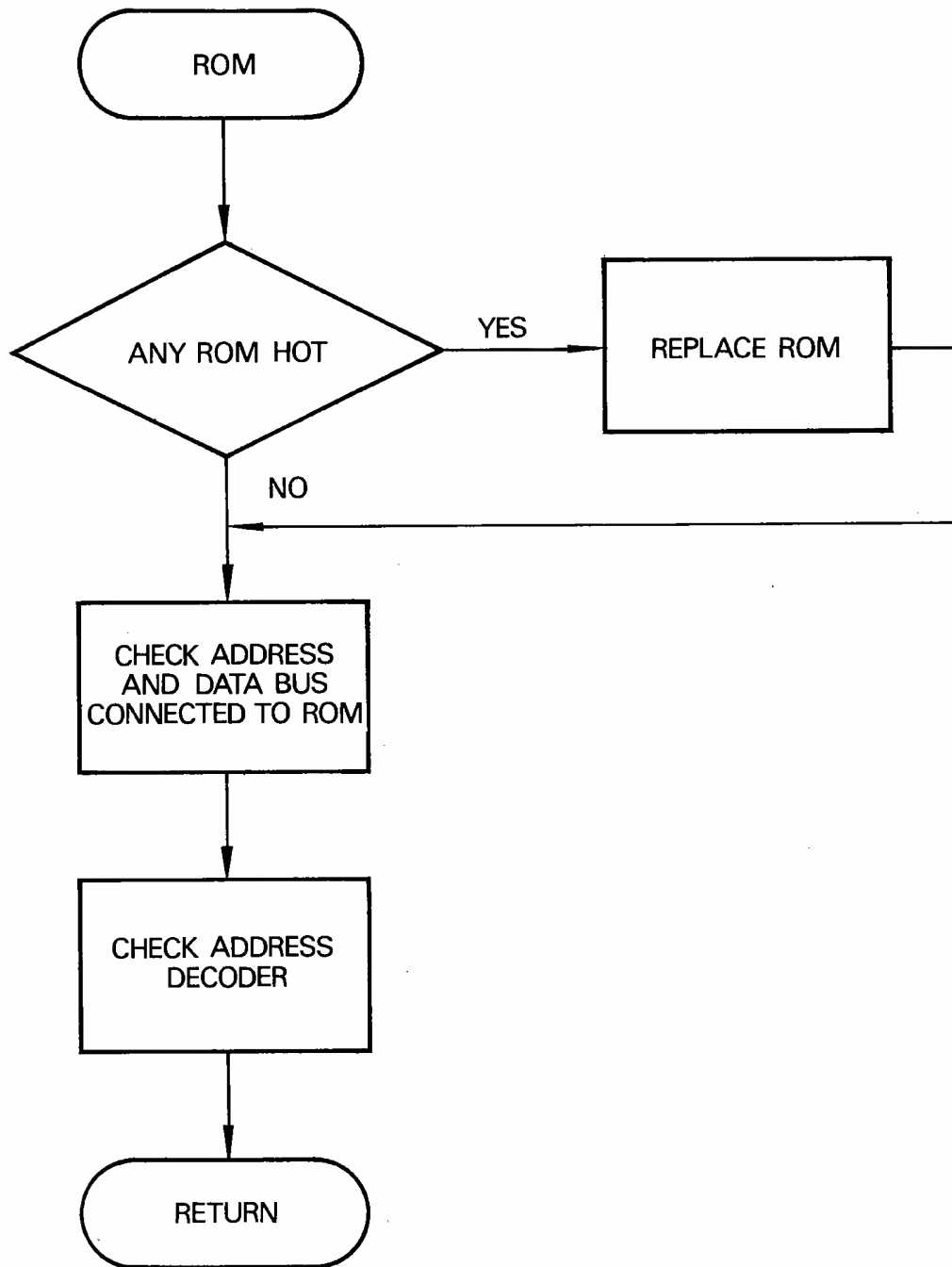2) If the display oscillates up and down, it may be due to low supply voltage. See whether there is any ripple at the 5V supply.

```
          ┌─────────────┐
          │     RAM      │
          └──────┬──────┘
                 │
                 ▼
        ┌─────────────────┐
        │  CHECK ADDRESS  │
        │     DECODER     │
        └────────┬────────┘
                 │
                 ▼
        ┌─────────────────┐
        │      CHECK      │
        │  MUX CAS RAS    │
        │     SIGNALS     │
        └────────┬────────┘
                 │
                 ▼
```

CHECK MUX CAS RAS (with overlines on MUX, CAS, RAS)

```
            ◇ ANY HOT RAM ◇ ──YES──▶ ┌──────────────┐
                 │                    │ REPLACE RAM  │
                 │                    └──────────────┘
                 │                           │
                 ◀───────────────────────────┘
                 ▼
        ┌─────────────────┐
        │ WHETHER THE RAM │
        │ PERFECTLY FITTED│
        │  INTO SOCKETS   │
        └────────┬────────┘
                 │
                 ▼
          ┌─────────────┐
          │   RETURN    │
          └─────────────┘
```
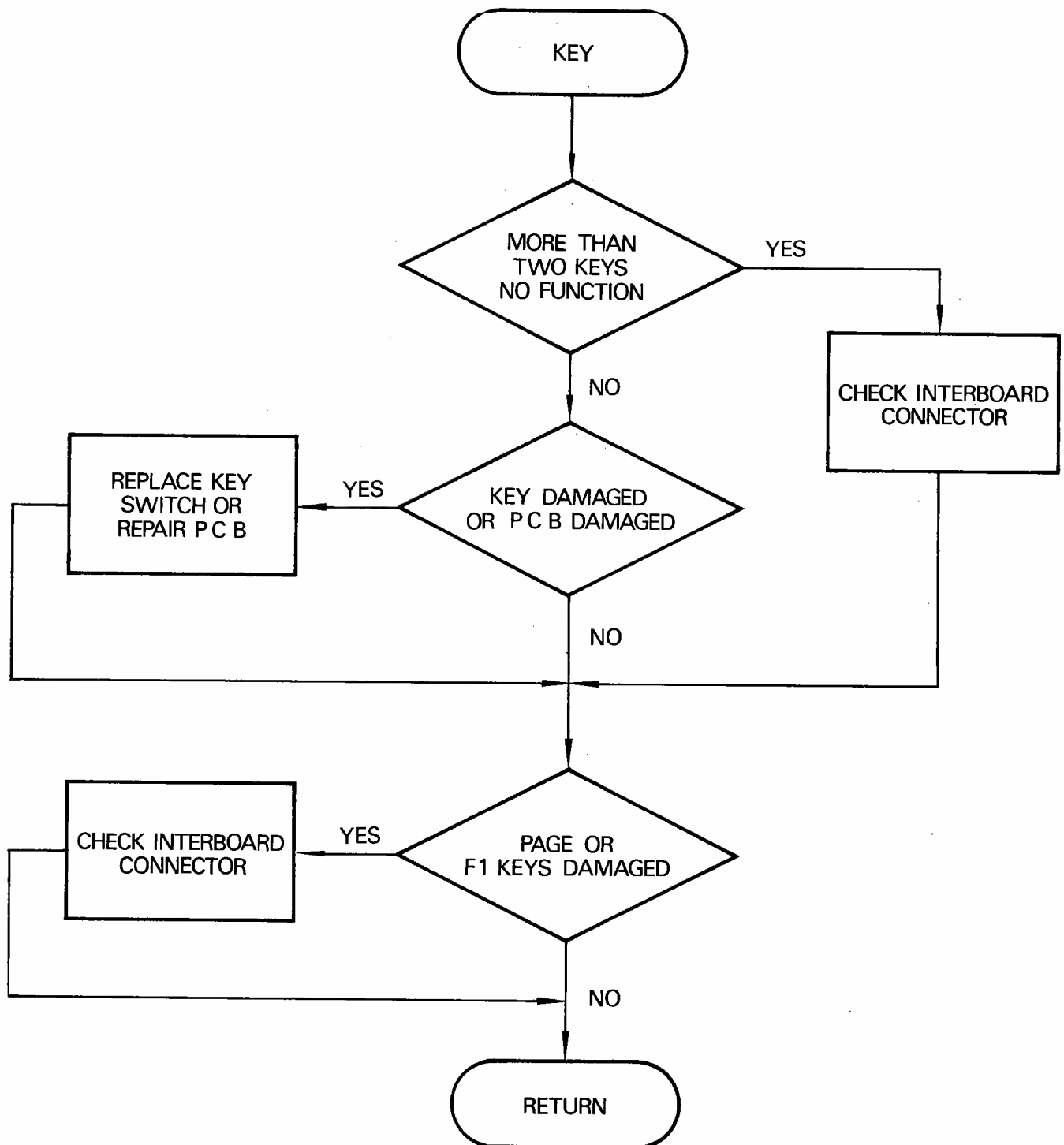
* Remark:—

The flowcharts of RAM and ROM checking seems quite simple, but it is most difficult to determine whether the component is damaged. The reason is that, if only one memory cell damaged, the machine cannot work properly or fails intermittently. The best way to check these sections is to replace the chips with good ones if other sections of the circuits are working perfectly.

Note:— CPU, RAM and ROM should be placed on conductive materials after taking out from the circuit.

```
              ┌──────────────┐
              │     ROM      │
              └──────┬───────┘
                     │
                     ▼
                  ╱──────╲
                 ╱        ╲         YES      ┌──────────────────┐
                ╱ ANY ROM  ╲─────────────────▶│   REPLACE ROM    │
                ╲   HOT    ╱                  └──────────────────┘
                 ╲        ╱                            │
                  ╲──────╱                             │
                     │ NO                              │
                     │◀────────────────────────────────┘
                     ▼
          ┌─────────────────────┐
          │   CHECK ADDRESS     │
          │   AND DATA BUS      │
          │ CONNECTED TO ROM    │
          └──────────┬──────────┘
                     │
                     ▼
          ┌─────────────────────┐
          │   CHECK ADDRESS     │
          │     DECODER         │
          └──────────┬──────────┘
                     │
                     ▼
              ┌──────────────┐
              │   RETURN     │
              └──────────────┘
```

```
                        ┌─────────────┐
                        │     KEY     │
                        └──────┬──────┘
                               │
                               ▼
                          ╱─────────╲
                         ╱ MORE THAN ╲        YES      ┌──────────────────┐
                         ╲ TWO KEYS   ╱───────────────▶│ CHECK INTERBOARD │
                          ╲NO FUNCTION╱                │    CONNECTOR     │
                           ╲─────────╱                 └──────────────────┘
                               │ NO
                               ▼
┌──────────────┐          ╱─────────╲
│ REPLACE KEY  │   YES   ╱ KEY DAMAGED╲
│ SWITCH OR    │◀───────╱ OR  P C B    ╲
│ REPAIR P C B │        ╲   DAMAGED    ╱
└──────────────┘         ╲─────────╱
                               │ NO
                               ▼
┌──────────────────┐      ╱─────────╲
│ CHECK INTERBOARD │ YES ╱ PAGE OR    ╲
│    CONNECTOR     │◀───╱ F1 KEYS      ╲
└──────────────────┘    ╲  DAMAGED     ╱
                         ╲─────────╱
                               │ NO
                               ▼
                        ┌─────────────┐
                        │   RETURN    │
                        └─────────────┘
```

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```
                              ┌─────────────┐
                              │     CAS     │
                              └──────┬──────┘
                                     │
                                     ▼
                              ╱──────────────╲
                             ╱    LOADING     ╲         NO
                            ╱  AND RECORDING OF ╲───────────────┐
                            ╲   CASSETTE 1 OK   ╱                │
                             ╲                 ╱                 │
                              ╲───────┬───────╱                  ▼
                                      │                   ╱───────────────╲      YES
                                      ▼                  ╱   REL 1  TURNED ON╲──────────┐
┌──────────────┐              ╱──────────────╲          ╲                   ╱           │
│ CHECK REL 2, │◄────────────╱    LOADING     ╲          ╲─────────┬───────╱            │
│   Q5, Q6     │             ╲  AND RECORDING OF╲                  │ NO                 │
└──────┬───────┘              ╲   CASSETTE 2 OK ╱                  ▼                    ▼
       │                       ╲               ╱            ┌──────────────┐    ┌──────────────┐
       │                        ╲──────┬──────╱             │ CHECK Q7,Q8,Z6,│   │ CHECK INTER- │
       │                          YES  │                    │  R28 AND Z9   │    │ CONNECTIONS  │
       │                               ▼                    └──────┬───────┘     └──────┬───────┘
       │               NO       ╱──────────────╲                   │                   │
       └──────────────────────╱  LOADING ERROR  ╲                  ▼                   │
                              ╲                  ╱           ┌──────────────┐           │
                               ╲────────┬───────╱            │CHECK CASSETTE│           │
                                        │                    │ADDRESS DECODER│           │
                                        ▼                    └──────┬───────┘           │
                               ┌──────────────┐                     │                   │
                               │CLEAN RECORDING│                    ▼                   │
                               │     HEAD     │                    ─────────────────────┘
                               └──────┬───────┘
                                      │
                                      ▼
                               ┌──────────────┐
                               │ CHECK OUTPUT │
                               │   AT Z9(1)   │
                               └──────┬───────┘
                                      │
                                      ▼
                              ┌─────────────┐
                              │   RETURN    │
                              └─────────────┘
```

Remark:—
     Sometimes, cassette loading error may not be caused by circuit fault, but due to poor quality of the
tape.

3. PICTURE POSITION ADJUSTMENT

After the video interface has been serviced, the picture position should be adjusted so as to place the picture in the centre of the screen.

Run the following program, a rectangle showing the screen boundary will then be drawn. Please adjust VR1 and VR2 with a non-metallic screw.

```
10    CLS
20    FOR X = 0 TO 127
30    SET (X, 0): SET (X, 47)
40    NEXT X
50    FOR Y = 0 TO 47
60    SET (0, Y): SET (63, Y): SET (64, Y): SET (127, Y)
70    NEXT Y
75    PRINT @ 522, "L E F T";: PRINT @ 554, "R I G H T",
80    GOTO 80
90    END
```

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4. SCHEMATIC DIAGRAMS

4.1 CPU BOARD – SHEET 1

VIDEO GENIE SYSTEM EG3003/4
MAIN BOARD SCHEMATIC DIAGRAM

SHEET 1

VIDEO GENIE SYSTEM EG3003/4
MAIN BOARD SCHEMATIC DIAGRAM
SHEET 2

4.3 INTERFACE BOARD – SHEET 1

VIDEO GENIE SYSTEM EG3003/4
INTERFACE CARD SCHEMATIC
DIAGRAM SHEET 1

4.4   INTERFACE BOARD – SHEET 2

VIDEO GENIE SYSTEM EG3003/4
INTERFACE CARD SCHEMATIC DIAGRAM SHEET 2
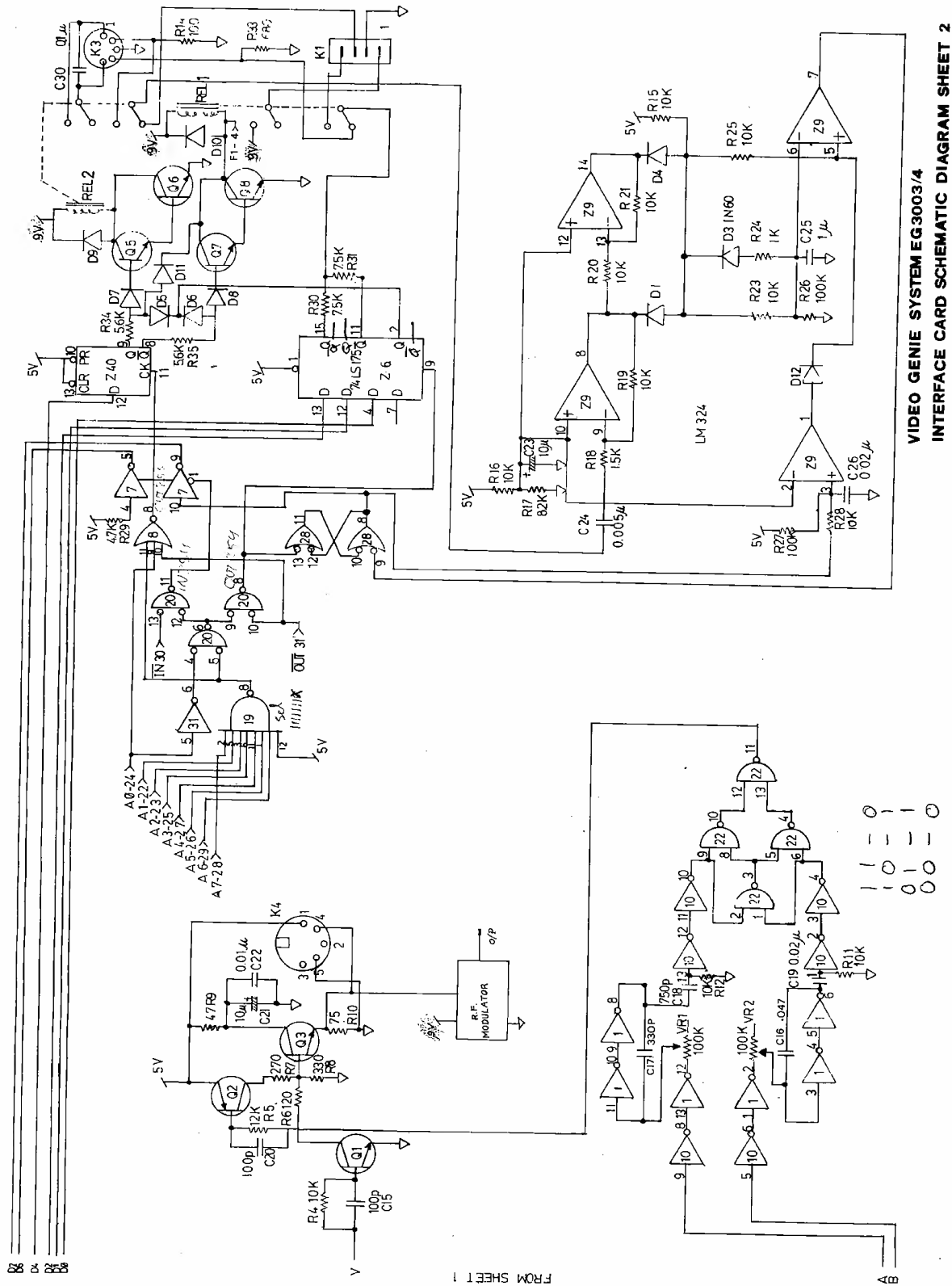
4.5 POWER SUPPLY AND KEYBOARD

POWER SUPPLY

KEYBOARD
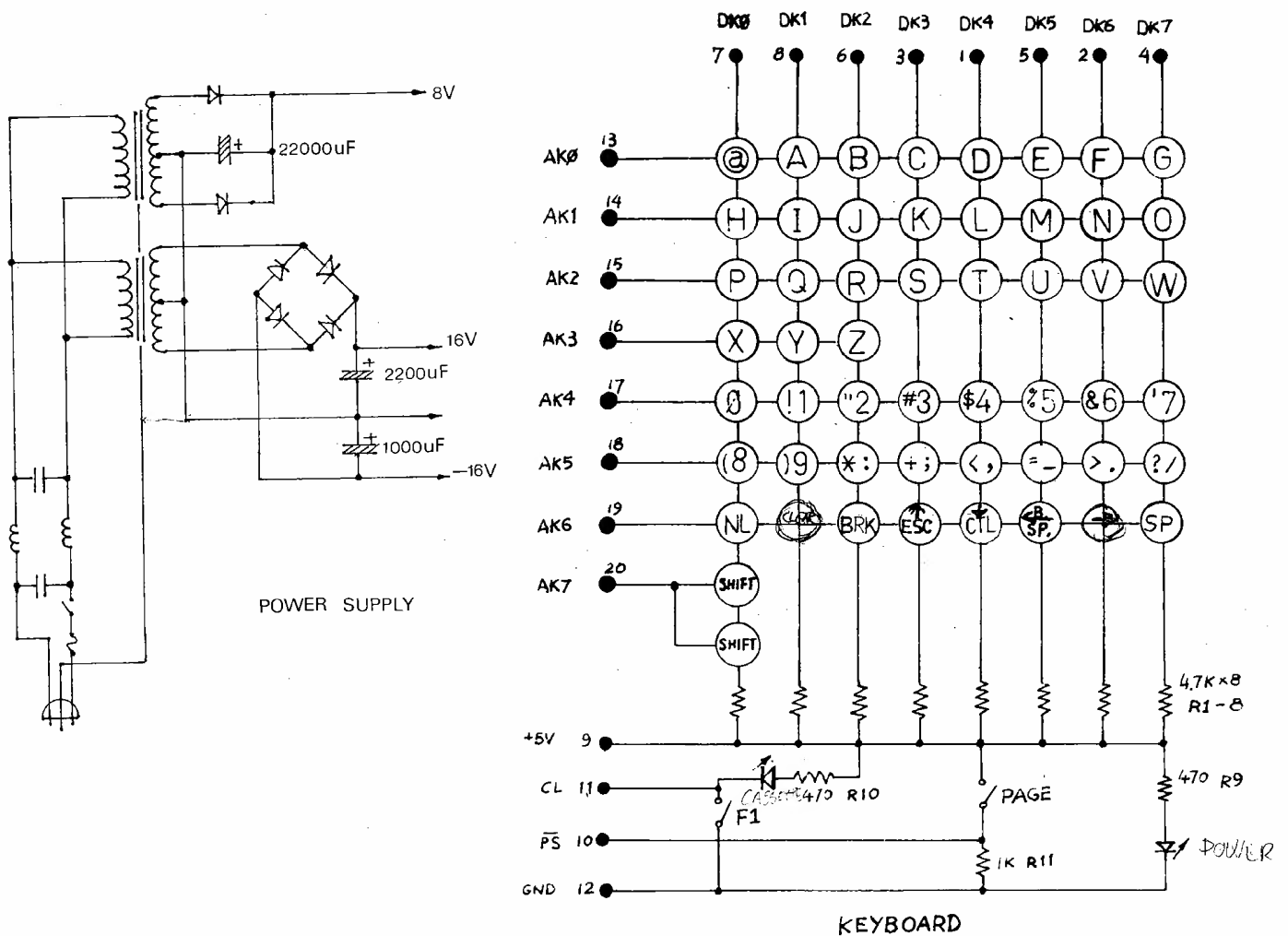
VIDEO GENIE SYSTEM EG3003/3004

4.6 CASSETTE RECORDER
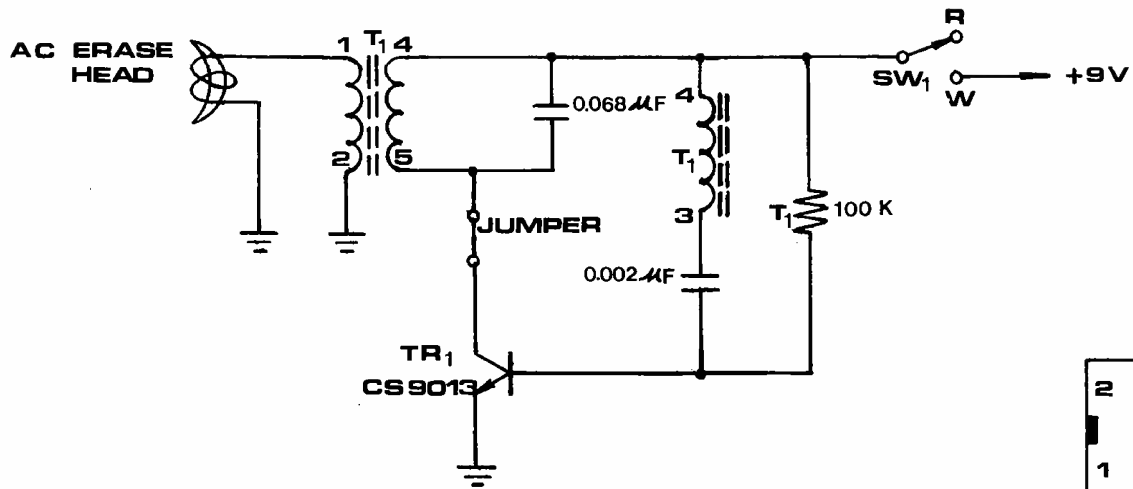
AC ERASE CIRCUIT
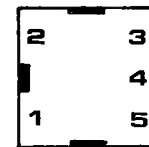
BOTTOM VIEW T₁
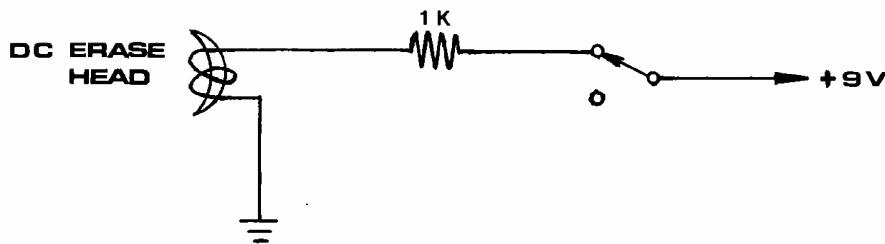
DC ERASE CIRCUIT
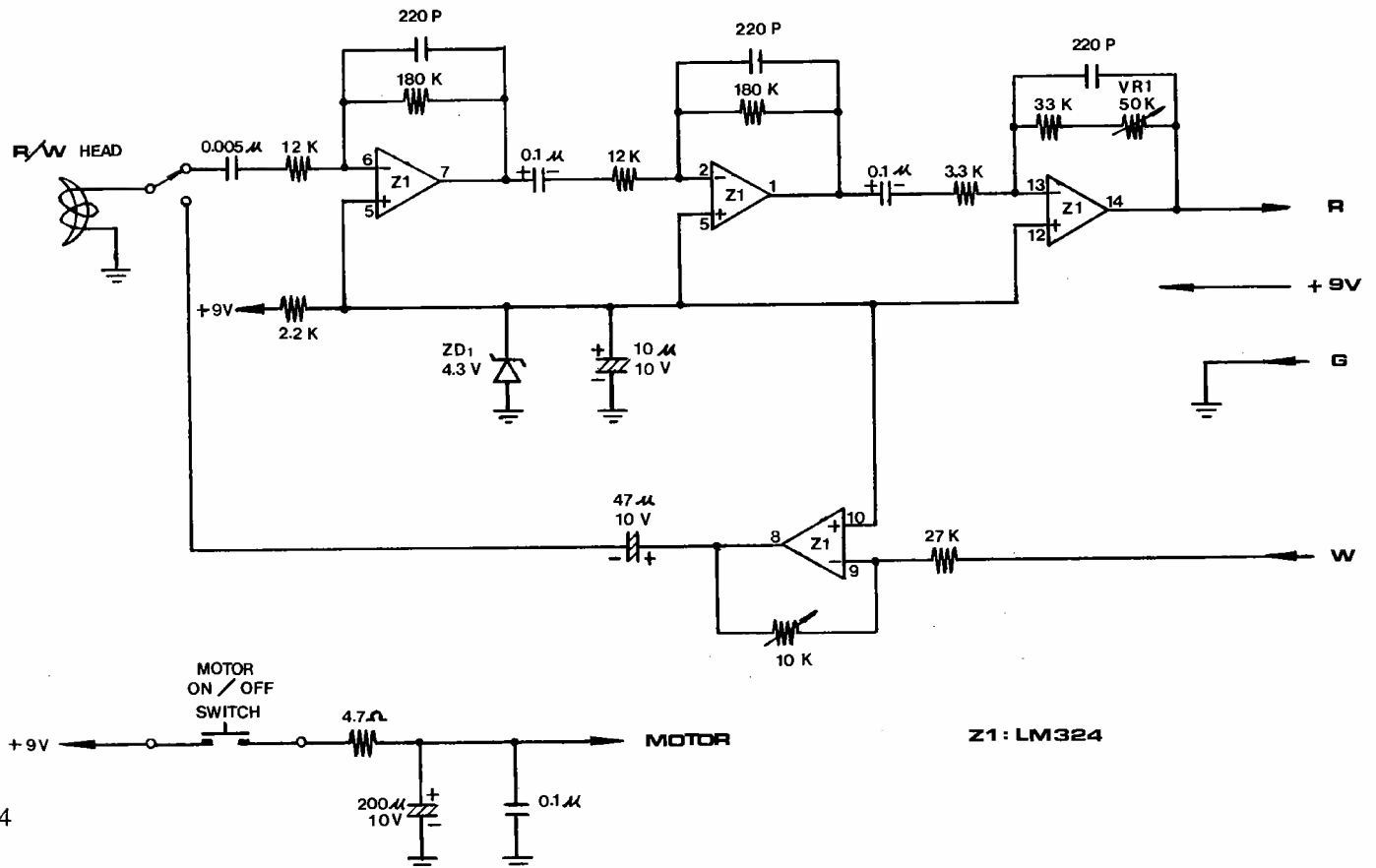
Z1: LM324

5. COMPONENT LAYOUT DIAGRAMS

5.1 CPU BOARD LAYOUT DIAGRAM

COMPONENT LAYOUT DIAGRAM
CPU BOARD
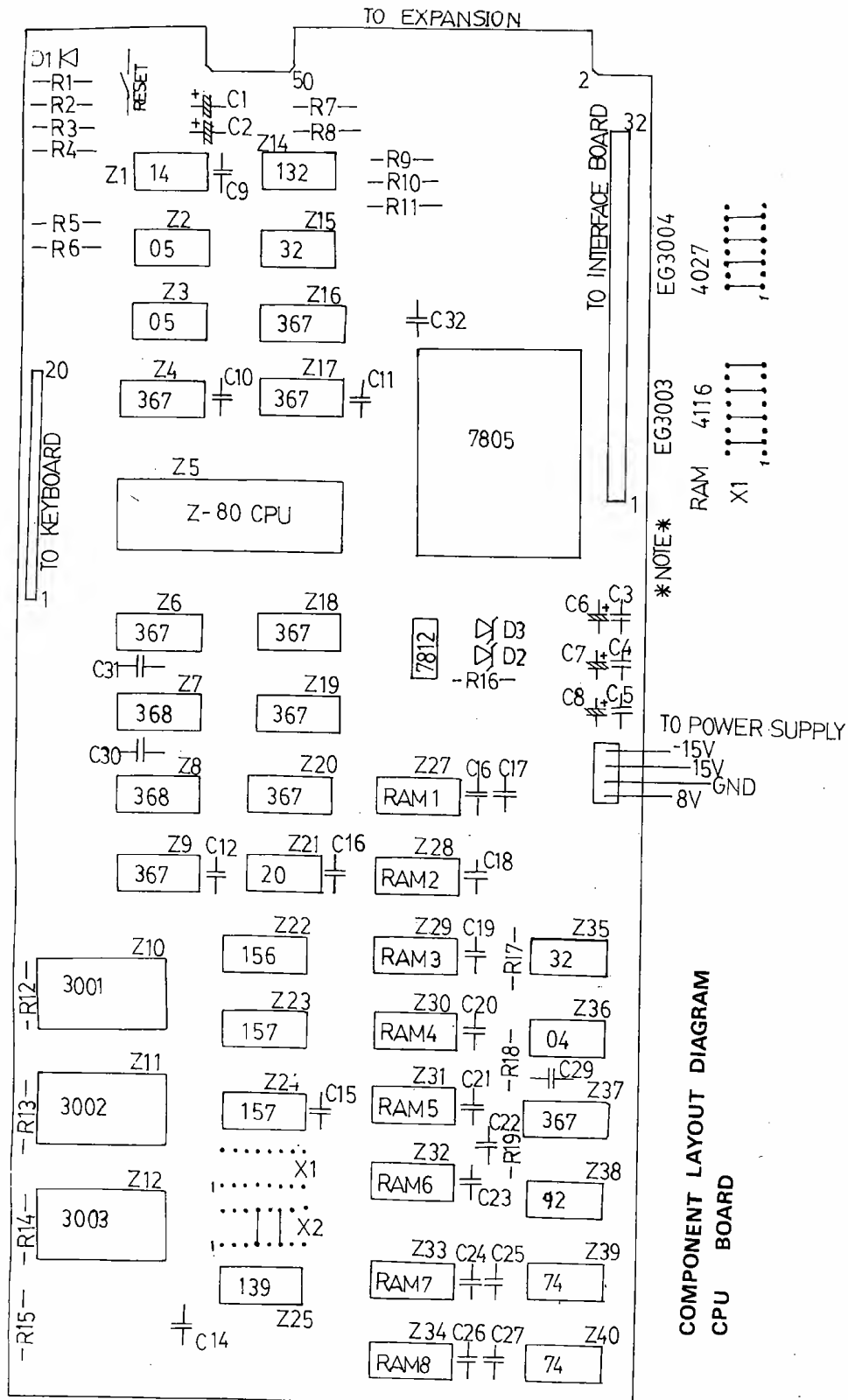
5.2 INTERFACE BOARD LAYOUT DIAGRAM

COMPONENT LAYOUT DIAGRAM
INTERFACE BOARD
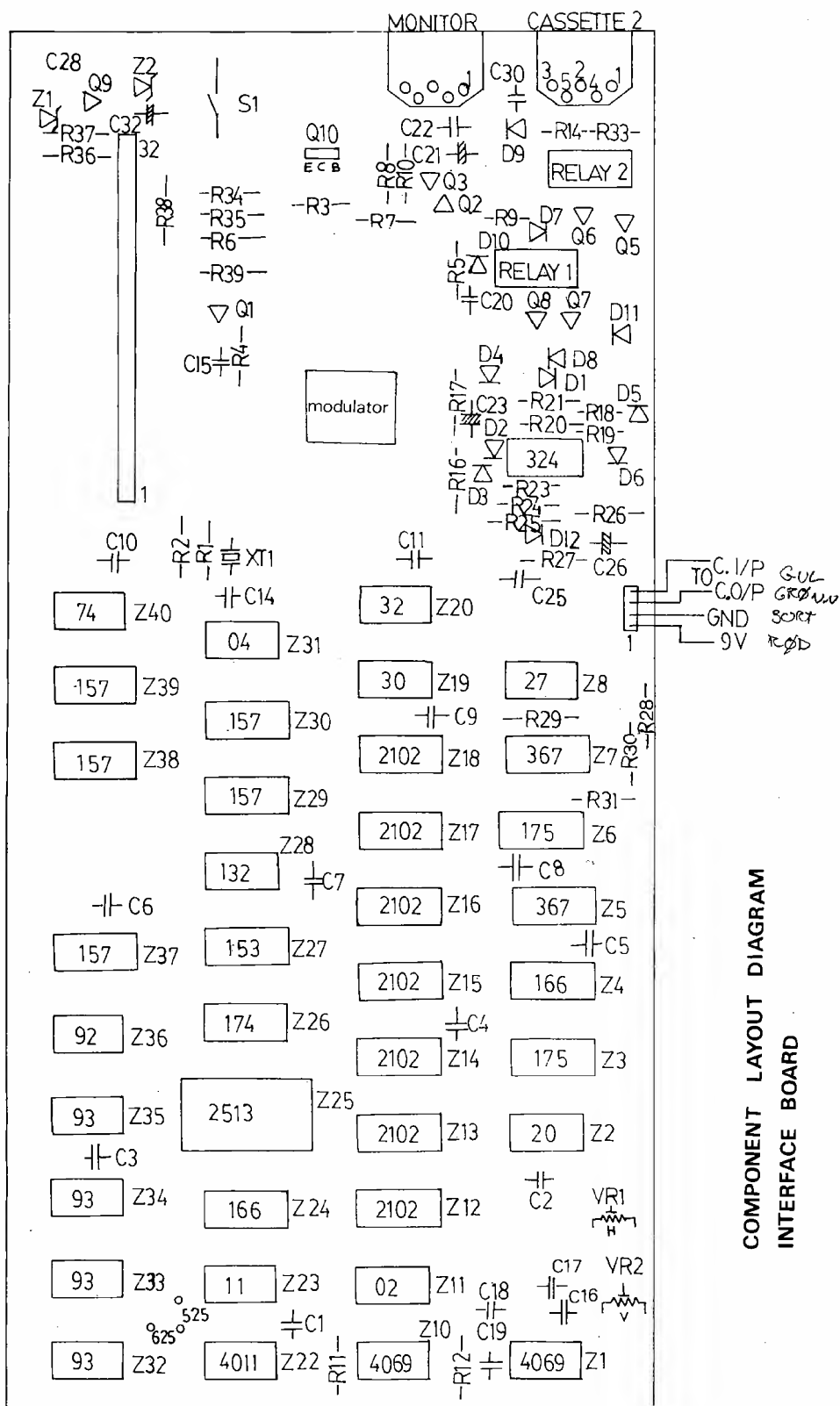
5.3   CASSETTE BOARD LAYOUT DIAGRAM
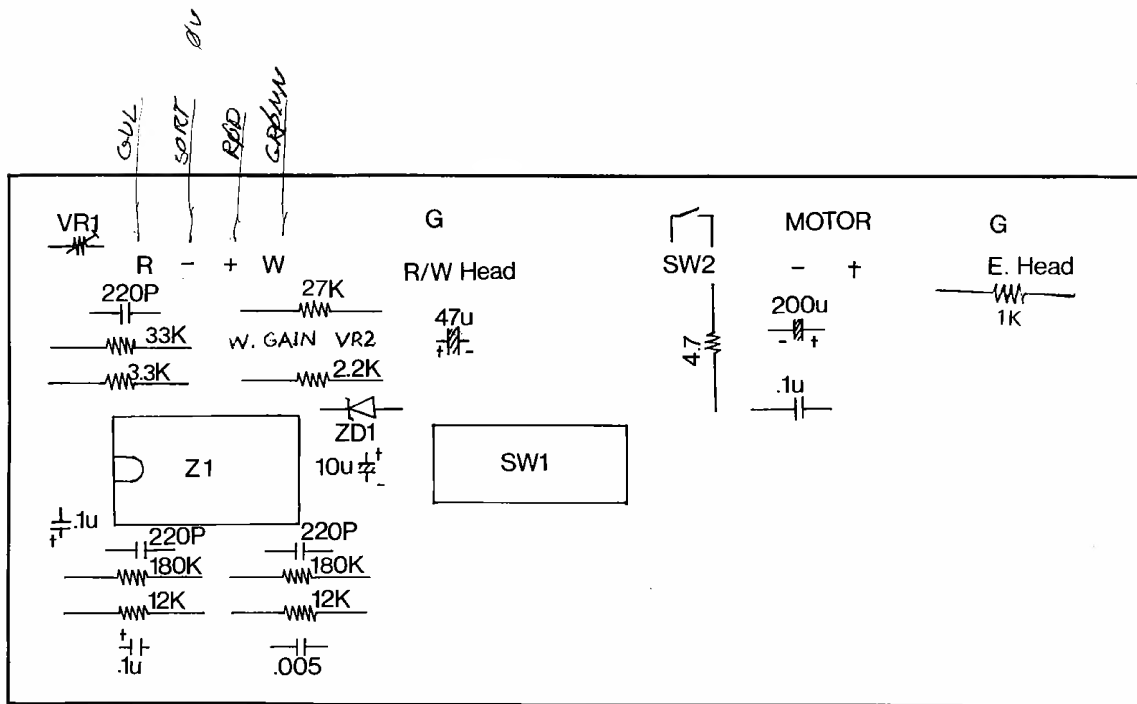
6. PIN ASSIGNMENTS OF CONNECTORS

6.1   PIN CONNECTIONS FOR EXPANSION INTERFACE

PIN	SIGNAL	PIN	SIGNAL
1	GND	26	A10
2	GND	27	A13
3	A7	28	A11
4	A6	29	A12
5	A5	30	PHI
6	A4	31	PINT
7	A1	32	NC
8	A3	33	NC
9	A2	34	PHLDA
10	A0	35	PHANTOM
11	D5	36	HALT
12	D2	37	PWAIT
13	NC	38	IORQ
14	D1	39	PHOLD
15	D0	40	WR
16	D3	41	RD
17	D7	42	CCDBS/STADBS
18	D6	43	MREQ
19	VCC	44	DODBS/ADDBS
20	D4	45	M1
21	A15	46	RESET
22	A8	47	RFSH
23	A14	48	NMI
24	A9	49	GND
25	NC	50	GND

EXPANSION PIN EDGE
VIEWED FROM REAR SIDE

```
2                            50
═══════════════════════════════
1                            49
```

SIGNAL EXPLANATION

PHI	1.79 MHz clock
PINT	INTERRUPT
NC	NO CONNECTION
PHLDA	PROCESSOR HOLD ACKNOWLEDGE
PHANTOM	PHANTOM
HALT	HALT ACKNOWLEDGE
PWAIT	PROCESSOR WAIT
IORQ	INPUT/OUTPUT REQUEST
PHOLD	PROCESSOR HOLD
WR	PROCESSOR WRITE
RD	PROCESSOR READ
CCDBS/STADBS	CONTROL AND STATUS BUS DISABLE
MREQ	MEMORY REQUEST
DODBS/ADDBS	DATA AND ADDRESS BUS DISABLE
M1	FIRST STATE OF INSTRUCTION CYCLE
RESET	CPU RESET
RFSH	DYNAMIC MEMORY REFRESH
NMI	NON-MASKABLE INTERRUPT

6.2   DIN CONNECTORS PIN ASSIGNMENTS

DIN JACK PIN CONNECTIONS FOR ADDITIONAL CASSETTE
1 —   REMOTE
2 —   SIGNAL GROUND
3 —   REMOTE
4 —   INPUT
5 —   OUTPUT

DIN JACK PIN CONNECTIONS FOR VIDEO INTERFACE
1 —   +5V
4 —   VIDEO OUTPUT
5 —   GROUND

DIN JACK VIDEO FROM REAR SIDE OF THE SYSTEM
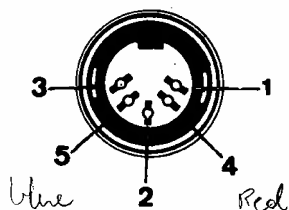
1   Red   in
2   Ground
3   Black   in
4   White   out
5   Yellow   out

6.3 INTER BOARD PIN CONNECTION

1	CK		17	D0
2	+15V		18	D1
3	PS		19	D5
4	CL		20	D2
5	WR		21	+5V
6	A11		22	A1
7	CK/2		23	A2
8	RD		24	A0
9	A10		25	A3
10	VID		26	A5
11	A9		27	A4
12	A8		28	A7
13	D4		29	A6
14	D6		30	IN
15	D7		31	OUT
16	D3		32	GND

PS — Page Select
CL — Cassette Local
VID — Video Ram Select

6.4   KEYBOARD, CPU BOARDS PIN CONNECTION

1	D4
2	D6
3	D3
4	D7
5	D5
6	D2
7	D0
8	D1
9	+5V
10	PS
11	CL
12	GND
13	A0
14	A1
15	A2
16	A3
17	A4
18	A5
19	A6
20	A7

7. DISASSEMBLY AND WIRING

To disassemble the Genie, firstly, unscrew eight screws at the bottom case; seven around the boundry and one at the middle. Secondly, take off two switch knobs at the back panel. Remove the top case and you will see the P.C.B.'s, power supply and cassette mounted on the bottom case.

After servicing the machine, remember to connect up the wires as shown in the wiring diagram.
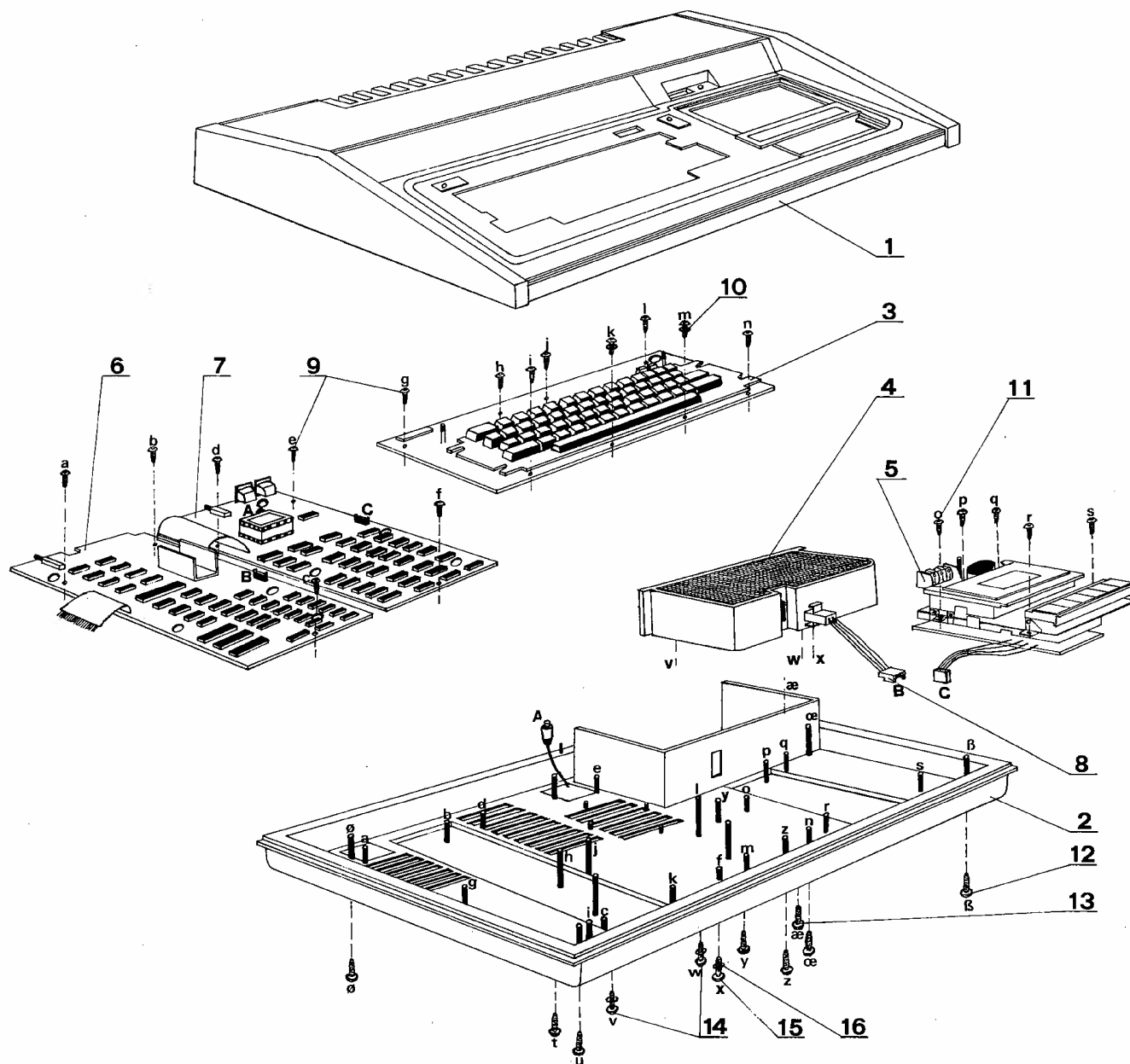
1- TOP CABINET
2- BOTTOM CABINET
3- KEY BOARD
4- POWER SUPPLY UNIT
5- CASSETTE
6- CPU BOARD
7- INTERFACE BOARD
8- POWER SUPPLY CABLE

9- SELF-TAPPING SCREW M3.5×8 〔14PCS.〕
10- PLAIN WASHER 3.5×0.5×8 〔2 PCS.〕
11- SELF-TAPPING SCREW M3 ×10 〔5PCS.〕
12- MACHINE SCREW M3×0.5×30 〔7PCS.〕
13- MACHINE SCREW M3×0.5×20 〔1PCS.〕
14- MACHINE SCREW M 3×0.5×22 〔1PCS.〕
15- MACHINE SCREW M 3×0.5×8 〔1PCS.〕
16- PLAIN WASHER   M 3.5×0.5×6 〔3PCS.〕

ASSEMBLY DIAGRAM

7.2   WIRING DIAGRAM

WIRING DIAGRAM
1. CPU-INTERFACE
   INTERCONNECTION CABLE
2. CPU-KEYBOARD
   INTERCONNECTION CABLE
3. ANTENNA COAXIAL CABLE
4. D.C. POWER CONNECTOR
5. CASSETTE CONNECTOR
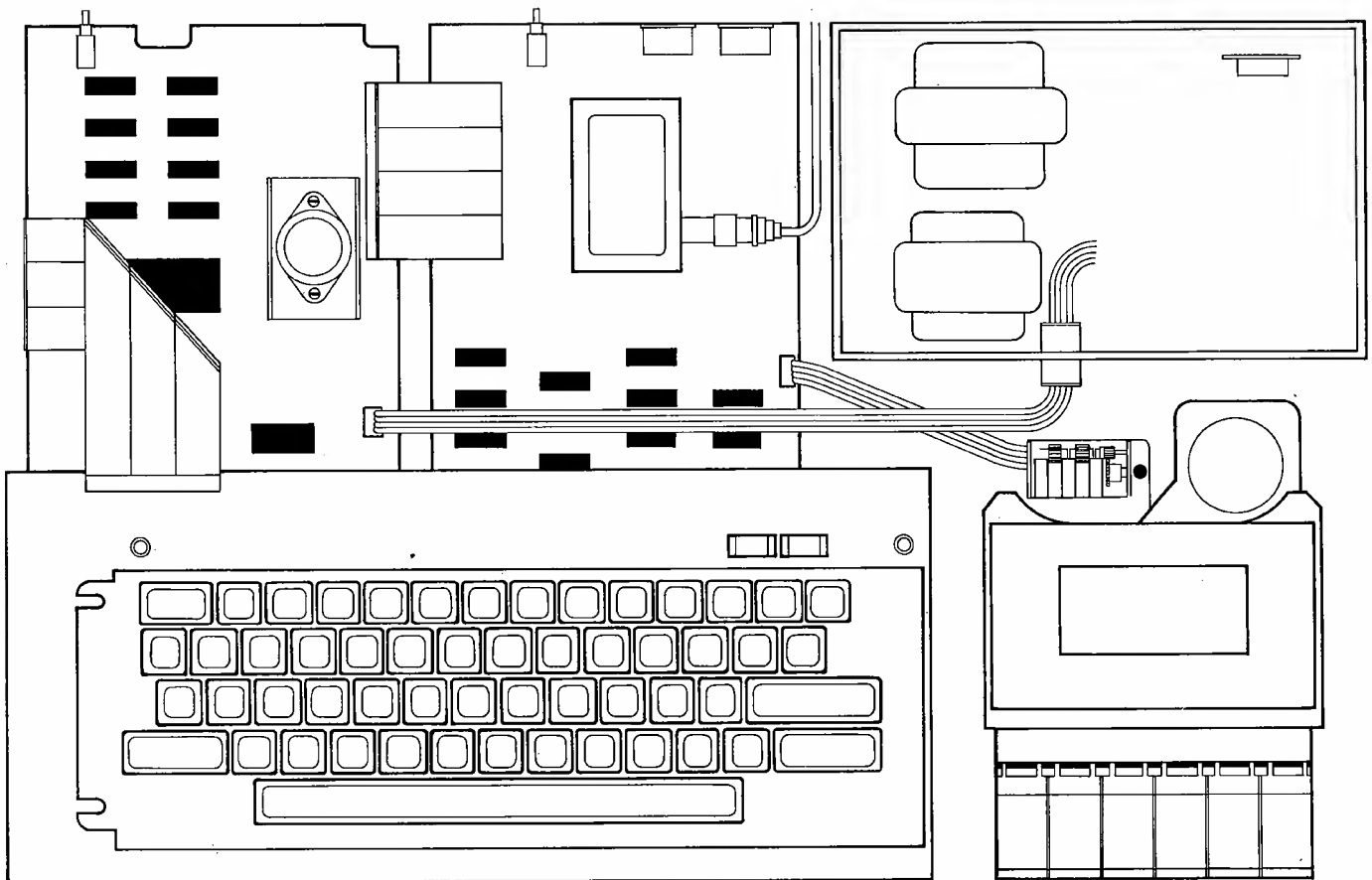
8. PART LIST

8.1 ** INTERFACE BOARD **

Symbol	Description	Part Number
	P.C.B.	48-3403002-00
Z1	4069	15-3040690-00
Z2	74LS20	15-2740202-00
Z3	74LS175	15-2741752-00
Z4	74LS166	15-2741662-00
Z5	74LS367	15-2743672-00
Z6	74LS175	15-2741752-00
Z7	74LS367	15-2743672-00
Z8	74LS27	15-2740272-00
Z9	LM324	16-2043530-00
Z10	4069	15-3040690-00
Z11	74LS02	15-2740022-00
Z12–18	21LS02	15-7021020-00
Z19	74L530	15-2740302-00
Z20	74LS32	15-2740322-00
Z22	4011	15-3040110-00
Z23	74LS11	15-2740112-00
Z24	74LS166	15-2741662-00
Z25	2513-001	15-3025130-00
Z26	74LS174	15-2741742-00
Z27	74LS153	15-2741532-00
Z28	74LS132	15-2441322-00
Z29, 30	74LS157	15-2740042-00
Z31	74LS04	15-2740042-00
Z32–35	74LS93	15-2740932-00
Z36	74LS92	15-2740922-00
Z37–39	74LS157	15-2741572-00
Z40	74LS74	15-2740742-00
R1, 2	1K (¼W)	21-2102220-00
R3	4.7K	21-2472220-00
R4, 5	10K	21-2103220-00
R6	120 ohm	21-2121220-00
R7	220 ohm	21-2221220-00
R8	330 ohm	21-2331220-00
R9	47 ohm	21-2470220-00
R10	75 ohm	21-2750220-00
R11, 12	10K	21-2103220-00
R14	120 ohm	21-2121220-00
R16, 17	10K	21-2103220-00
R18	1.5K	21-2152220-00
R19	15K	21-2153220-00
R20, 21	10K	21-2103220-00
R23	10K	21-2103220-00
R24	1K	21-2102220-00
R25	10K	21-2103220-00
R26, 27	100K	21-2104220-00
R28	10K	21-2103220-00

Symbol	Description	Part Number
R29	4.7K	21-2472220-00
R30, 31	10K	21-2103220-00
R33	680 ohm	21-2681220-00
R34,35	4.7K	21-2472220-00
R36	1K	21-2102220-00
R37, 38	560 ohm	21-2561220-00
R17	8.2K	21-2822220-00
VR1, 2	100K Semivarible	22-5104101-00
REL1, 2	9V Relay	42-1223001-00
C1–12	0.1 uF Ceramic	25-1104430-00
C14	220 pF Ceramic	25-1221430-00
C15	100 pF Ceramic	25-1101430-00
C16	0.05 uF Ceramic	25-1503430-00
C17	330 pF Ceramic	25-1331430-00
C18	750 pF Ceramic	25-1751430-00
C19	0.022 uF Mylar	25-2223220-00
C20	100 pF Ceramic	25-1101430-00
C22	0.1 uF Ceramic	25-1104430-00
C23	10 uF 16 V Electrolytic	26-3106430-00
C24	0.005 uF Ceramic	25-1502430-00
C25	1 uF 10 V Electrolytic	26-3105420-00
C26	0.022 uF Mylar	25-1104430-00
C30, 31	0.1 uF Ceramic	25-1104430-00
C32	10 uF 16 V Electrolytic	26-3106430-00
Q1	9018G	11-1901830-00
Q2	9015A	11-1901500-00
Q3	9018G	11-1901830-00
Q5–9	9013G	11-1901330-00
Q10	NA51W	11-1005110-00
D1–4	IN60	12-3006000-00
D5–12	IN4148	12-2414800-00
D13	8.2V Zener	12-5820051-01
C21	100 uF 10 V Electrolytic	26-3107420-00
C28	100 uF Electrolytic	26-3107420-00
	10.644 MHz Xtal	31-1106441-00
	5 pin Din Jack	43-1300501-00
	Push button locked switch	41-2227170-00
	4 pin terminal	43-7916070-00
	16 pin wiremate flat cable	44-7916070-00
	24 pin IC socket	43-2202401-00
	Modulator UHF CH36	16-5053600-00
	Modulator VHF AUS. CH1	16-5050100-00
	Modulator VHF USA CH3	16-5051180-00
	Modulator CCIR CH3	16-5050300-00

*** Part List ***

8.2   ** CPU BOARD **

Symbol	Description	Part Number
	P.C.B.	48-3403001-00
Z1	74LS14	15-2740142-00
Z2	74LS05	15-2740052-00
Z3	74LS05	15-2740052-00
Z4	74LS367	15-2743672-00
Z5	Z80 CPU	15-6000800-00
Z6	74LS367	15-2743672-00
Z7, 8	74LS368	15-2743682-00
Z9	74LS367	15-2743672-00
Z10	9332B E3001	15-8030010-00
Z11	9332B E3002	15-8030020-00
Z12	9332B E3003	15-8030020-00
Z14	74LS132	15-2741322-00
Z15	74LS32	15-2740322-00
Z16−20	74LS367	15-2743672-00
Z21	74LS20	15-2740202-00
Z22	74LS156	15-2741562-00
Z23, 24	74LS157	15-2741572-00
Z25	74LS139	15-2741392-00
Z27−34	*4116	15-7041160-00
Z35	74LS32	15-2740322-00
Z36	74LS04	15-2740042-00
Z37	74LS367	15-2743672-00
Z38	74LS92	15-2740922-00
Z39, 40	74LS74	15-2740742-00
C1	10 uF 16 V Electrolytic	26-3106430-00
C2	100 uF 10 V Electrolytic	26-3107420-00
C3−5	0.1 uF Ceramic	25-1104430-00
C6−8	10 uF 16 V Electrolytic	26-3106430-00
C9−27	0.1 uF Ceramic	25-1104430-00
C30, 31	0.1 uF Ceramic	25-1104430-00
R1−15	4.7K (¼W)	21-2472220-00
R16	2K	21-2202230-00
R17, 18	4.7K	21-2472220-00
R19	1.8K	21-2182240-00
D1	IN 4148	12-2414800-01
D2	IN 5231 (5.1 V Zener)	12-5523100-00
D3	IN 4735 (6.2 V Zener)	12-5473500-00
	16 pin IC sockets	43-2201601-00
	24 pin IC sockets	43-2202401-00
	40 pin IC sockets	43-2204001-00
	7805 (TO-3)	16-2780560-00
	7812 (TO-220)	16-1781290-00
	Push button switch	41-2227150-00
	4 pin terminal	43-7200402-00
	16 pin wiremate receptacle	43-9201601-00
	20 pin wiremate flat cable	44-7920130-00

8.3   ** POWER SUPPLY **

Description	Part Number
IN4001	12-1400100-00
IN5400	12-1540000-00
2,200 uF 25 V Elec. Cap.	26-4228444-00
22,000 uF 16 V Elec. Cap.	26-4229443-00
1,000 uF 25 V Elec. Cap.	26-3108444-00
0.02 uF 1 KV Ceramic Cap.	25- 1203400-00
0.1 uF Ceramic Cap.	25-1104430-00
20 uH choke	38-5020111-00
P.C.B.	48-1003001-00
Fuse (1A)	46-0102020-00
Fuse (0.5A)	46-0501020-00
Fuse holder	51-4070010-00
4 pin connecting plug	43-7100451-00
Rocker Switch	41-7129401-00
117 V : 9.6 V x 2 transformer	36-1110201-00
220 V : 9.6 V x 2 transformer	36-1410201-00
220 V : 9.6 V x 2 transformer	36-1115061-00
117 V : 15 V x 2 transformer	36-1115061-00
220 V : 15 V x 2 transformer	36-1315062-00
240 V : 15 V x 2 transformer	36-1415061-00

8.4   ** KEYBOARD **

Description	Part Number
P.C.B.	48-2003003-00
LED	13-1592010-00
20 pin wiremate receptacle	43-9202001-00
1K Resistor (¼W)	21-2102220-00
470 ohm (¼W)	21-2471220-00
4.7 K (¼W)	21-2472220-00
Keyswitches	41-6120100-00
Keyswitches	41-6120101-00
Keyswitches	41-6120102-00
Locked Switch	41-2120103-00
Dummy Key	63-9503000-00
Spring	63-7203000-00
Space bar accessories	62-9103000-00
Space bar accessories	62-9103001-00
Space bar accessories	62-8103000-00
Space bar accessories	63-5203000-00
Shift & newline accessories	62-9103003-00
Shift & newline accessories	62-9103004-00
Keytops 1	57-1203000-00
Keytops 2"	56-1203001-00
Keytops 3	57-1203002-00
Keytops 4$	56-1203003-00
Keytops 5%	56-1203004-00
Keytops 6&	57-1203005-00
Keytops 7'	57-1203006-00
Keytops 8(	57-1203007-00
Keytops 9)	57-1203008-00
Keytops 0	57-1203009-00
Keytops *:	57-1203010-00
Keytops —=	57-1203011-00
Keytops @	57-1203012-00
Keytops +;	57-1203013-00
Keytops A	57-1203014-00
Keytops B	57-1203015-00
Keytops C	57-1203016-00
Keytops D	57-1203017-00
Keytops E	57-1203018-00
Keytops F	57-1203019-00
Keytops G	57-1203020-00
Keytops H	57-1203021-00
Keytops I	57-1203022-00
Keytops J	57-1203023-00
Keytops K	56-1203024-00
Keytops L	57-1203025-00
Keytops M	57-1203026-00
Keytops N	57-1203027-00

Description	Part Number
Keytops O	57-1203028-00
Keytops P	57-1203029-00
Keytops Q	57-1203030-00
Keytops R	57-1203031-00
Keytops S	57-1203032-00
Keytops T	57-1203033-00
Keytops U	57-1203034-00
Keytops V	57-1203035-00
Keytops W	57-1203036-00
Keytops X	57-1203037-00
Keytops Y	57-1203038-00
Keytops Z	57-1203039-00
Keytops SHIFT	57-1203040-00
Keytops ,	57-1203041-00
Keytops .	56-1203042-00
Keytops ?/	57-1203043-00
Space Bar	57-1203044-00
Page	57-1203045-00
F1	57-1203046-00
CTRL	57-1203047-00
BACKSPACE	57-12o3048-00
NEWLINE	56-1203049-00
BREAK	57-1203050-00
ESC	57-1203051-00

8.5   **CASSETTE BOARD**

Description	Part number
4.3V zener diode	12-5032400-00
LM324	16-1032420-00
1K	21-2102220-00
12K	21-2123220-00
180K	21-2184220-00
2.2K	21-2222220-00
27K	21-2273220-00
3.3K	21-2332220-00
33K	21-2333220-00
4.7 ohm	21-2479220-00
10K semivarible resistor	22-5103101-00
50K semivarible resistor	22-5503101-00
0.1 μF Ceramic	25-1104430-00
220P Ceramic	25-1221220-00
0.005 μF Ceramic	25-1502430-00
0.1 μF Aluminium	26-1104320-00
10 μF 10V Elec.	26-3016420-00
200 μF 10V Elec.	26-3207420-00
47 μF 10V Elec.	26-3476420-00
2P2T slide switch	41-1226102-00
Connector E5051M	43-7100401-00
PCB	48-1003002-00
Audio cassette recorder	71-2200001-00
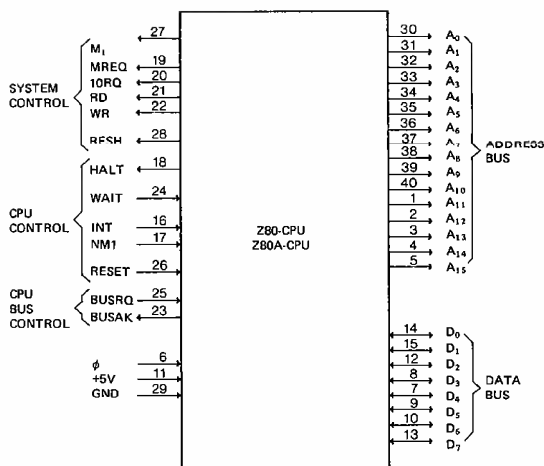
Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus)	Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D_0-D_7 (Data Bus)	Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M_1}$ (Machine Cycle one)	Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{MREQ}$ (Memory Request)	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
$\overline{IORQ}$ (Input/ Output Request)	Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.
$\overline{RD}$ (Memory Read)	Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{WR}$ (Memory Write)	Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{RFSH}$ (Refresh)	Output active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.
$\overline{HALT}$ (Halt state)	Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.
$\overline{WAIT}$ (Wait)	Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.
$\overline{INT}$ (Interrupt Request)	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.
$\overline{NMI}$ (Non Maskable Interrupt)	Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.
$\overline{RESET}$	Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.
$\overline{BUSRQ}$ (Bus Request)	Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state to that other devices can control these busses.
$\overline{BUSAK}$ (Bus Acknowledge)	Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later MREQ goes active. The falling edge of MREQ can he used directly as a chip enable to dynamic memories. RD when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal RFSH indicates that a refresh read of all dynamic memories should be accomplished.

MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The MREQ and RD signals are used exactly as in the fetch cycle. in the case of a memory write cycle, the MREQ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The WR line is active when data on the data bus is stable to that it can be used directly as a R/W pulse on virtually any type of semiconductor memory.

INPUT OR OUTPUT CYCLES

Illustration here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and active the WAIT line if a wait is required.

INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the IORQ signal becomes active (instead of MREQ) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.